DRC Short Course - Best Practices for Reporting on Electronic Devices – Sunday, June 21, 2026

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"Best Practices in Reporting and Benchmarking Performance of 2D Transistors: A Scaling and Contacts Story"

Dr. Aaron Franklin is the Edmund T. Pratt, Jr. Distinguished Professor at Duke University, where he is also the Associate Dean for Faculty Affairs in the Pratt School of Engineering. Dr. Franklin received his Ph.D. in Electrical Engineering from Purdue in 2008 and then spent six years on the research staff at IBM. In 2014, he joined the faculty at Duke where his group explores the use of 1D and 2D nanomaterials for high-performance nanoscale devices, low-cost printed and recyclable electronics, and biomedical sensing systems. Dr. Franklin has been actively involved in the translation of inventions out of the lab, holding more than 50 issued patents and being engaged in two funded start-ups, one of which was acquired by a Fortune 500 company. He is a fellow of the IEEE and NAI and has published more than 120 scientific papers in the field of nanomaterial-based electronics.

Abstract:

The most significant obstacle facing 2D semiconductor-based transistors may not be the synthesis of large-area, defect-free crystals or the consistent realization of perfect contact interfaces (though, both would be ideal). Rather, the primary challenge may be determining how much real progress has been made amid the vast landscape of thousands of scientific papers. For 2D semiconductors to be viable in high-performance, aggressively scaled digital transistors, key device metrics must be carefully benchmarked against target specifications for future technology nodes. The list of metrics presented in the IEEE International Roadmap for Devices and Systems (IRDS) can be overwhelming and, when read properly, does include more commonly reported values such as on-current, subthreshold swing, contact resistance, and operating voltage. Given the broad and interdisciplinary nature of this research community, unintentional errors in extracting or interpreting these parameters can occur, leading to misleading claims or, at minimum, inconsistent reporting standards.

This tutorial will review the critical performance metrics used to evaluate 2D transistors and highlight common pitfalls in their extraction and reporting. It will be shown how, at the device level, the long-term viability of 2D transistors for high-performance technologies depends largely on proper electrostatic scaling, scalability, and the structure and performance of the contacts. Recent progress in understanding and engineering contact interfaces will be discussed in the context of meeting the requirements of future transistor technology nodes.