2024
DESIGN AND VERIFICATION™
DVCON
CONFERENCE AND EXHIBITION
UNITED STATES

SAN JOSE, CA, USA
MARCH 4-7, 2024

DVCON 2024 UNITED STATES CONFERENCE PROGRAM

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2024 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

DVCon U.S. 2024



Welcome Message from DVCon U.S. General Chair, Tom Fitzpatrick

General Chair – Tom Fitzpatrick, Siemens EDA

Welcome to DVConUS 2024! This is our 36th year as the premier Design and Verification Conference and Exhibition – the must-attend conference for the practicing design and verification engineer. As conference General Chair, on behalf of the Steering Committee, I would like to thank you for taking time out of your busy professional and personal life to be with us this week. Whether you've come to see some of the outstanding technical presentations and posters, visit with our many exhibitors to see the latest tools, technologies and services from the best companies in the industry, attend the panel discussion and keynote sessions, or just attend the sponsored lunches and evening cocktail receptions to renew old acquaintances and make new friends, we are so happy that you are here. I'm sure you'll find this week to be one of the highlights of your year.

Our tutorials and workshops on Monday and Thursday will cover many important topics from Portable Stimulus, Functional Safety, RISC-V design and verification, and Low-power verification to Network-on-Chip optimization, Clock/Reset Domain Crossing and Static Signoff, Large Language Model code generation and Chiplets. The main technical sessions on Tuesday and Wednesday will feature 42 paper presentations on everything from Coverage, Formal and Mixed-Signal design and verification to Verification Planning and Regression Management, UVM and SystemVerilog verification techniques and Artificial Intelligence and Machine Learning. We'll also have over 20 posters on an even wider array of topics. I'd like to thank all of the authors who submitted abstracts, papers and posters. We wouldn't have a program without you. In particular, I'd like to thank Josh Rensch, our Technical Program Chair, and Dave Rich, Vice-Chair, as well as the members of the Technical Program Committee, for all the work they did in putting this amazing program together. If you run into anyone with a "Technical Committee" ribbon on their badge, please be sure to say "thank you."

We're expanding our Keynote presentations this year to provide a wider perspective than just what to expect in EDA. Our Tuesday keynote presentation will feature Paul Cunningham, Senior VP/GM at Cadence, and a special guest from a user who will help you see how the chip you're working on may impact more than just the box it's going in. This year, we're also adding a second Keynote presentation on Wednesday from Alex Starr, AMD Corporate Fellow, who will share his insights as well. Alex is a long-time DVCon supporter and attendee, so we're very grateful that he will be such an important part of the program this year.

In addition to the technical sessions, Wednesday will kick off with a great panel discussion on "When Will We Be Able to Say, 'EDA-GPT, Verify My ASIC'?." In the words of Douglas Adams from The Hitchhiker's Guide to the Galaxy, Don't Panic! Come listen to our panel of experts give their thoughts on what our jobs may look like in a few years (or less).

We're also bringing back the Poster Ninja Warrior session, which will include four posters battling it out for top honors on Wednesday. Each Poster Warrior will be given five minutes to present their poster, followed by an insightful Q&A from a panel of expert judges. Audience reaction is encouraged and is an integral part of the judging process, creating a dynamic and interactive event.

I would like to express my gratitude to our program sponsor, Accellera Systems Initiative, our industry sponsors, my fellow members of the Steering Committee, and the Conference Catalyst staff who have worked so hard to put together a program that makes DVConUS the conference for design and verification engineers.

I sincerely hope to see you at DVConUS 2024.

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CONFERENCE SPONSOR



Accellera Systems Initiative is an independent, not-for profit organization dedicated to create, support, promote, and advance system-level design, modelling, and verification standards for use by the worldwide electronics industry. We are composed of a broad range of members that fully support the work of our technical committee to develop technology standards that are balanced, open, and benefit the worldwide electronics industry. Leading companies and semiconductor manufacturers around the world are using our electronic design automation (EDA) and intellectual property (IP) standards in a wide range of projects in numerous application areas to develop consumer, mobile, wireless, automotive, and other "smart" electronic devices. Through an ongoing partnership with the IEEE, standards and technical implementations developed by Accellera Systems Initiative are contributed to the IEEE for formal standardization and ongoing governance.

Our Mission

At Accellera our mission is to provide a platform in which the electronics industry can collaborate to innovate and deliver global standards that improve design and verification productivity for electronics products.

The purposes of the organization include:

- Provide design and verification standards required by systems, semiconductor, IP, and design tool companies to enhance a front-end design automation process.
- Collaborate with our community of companies, individuals, and organizations to deliver standards that lower the cost of designing commercial IC and EDA products and embedded system solutions, as well as increase the productivity of designers worldwide.
- Encourage availability and adoption of next-generation EDA and IP standards that encompass system-level, RT-level, and gate-level design flows.
- Collaborate with the electronic design community to deliver standards that increase designer productivity and lower the cost of product development.
- Provide mechanisms that enable the continued growth of the Accellera Systems Initiative user community including SystemC, Universal Verification Methodology (UVM), and IP-XACT.
- Standardize technical implementations developed by Accellera Systems Initiative through the IEEE
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DVCon U.S. 2024 - Program Grid
4 March 2024

TIME (PST)	Monterey Carmel	Oak	Fir	Bayshore Ballroom
9:00 - 10:30	**Portable Stimulus** accellera SYSTEMS INITIATIVE	**USF-based FMEDA-driven Functional Safety Verification** cadence	**IP-XACT** accellera SYSTEMS INITIATIVE	
10:30 - 11:00	**Coffee Break** (Gateway Foyer)			
11:00 - 12:30	**Portable Stimulus (continued)** accellera SYSTEMS INITIATIVE	**USF-based FMEDA-driven Functional Safety Verification (continued)** cadence	**Hierarchical CDC and RDC closure with standard abstract models** accellera SYSTEMS INITIATIVE	
12:30 - 13:30	**Lunch Sponsored by:** accellera SYSTEMS INITIATIVE (Pine Cedar)			
13:30 - 15:00	**Automatic generation of Device Driver and Programmer's Reference Manual from PSS** AGNISYS SYSTEM DEVELOPMENT WITH CERTAINTY	**Streamlining Low-Power Verification: From UPF to Signoff** SYNOPSYS	**Functional Safety** accellera SYSTEMS INITIATIVE	**Exhibitor Set Up**
15:00 - 15:30	**Coffee Break** (Gateway Foyer)			
15:30 - 17:00	**UVM Update & A Practical Guide to SA-EDI Methodology SystemC Sneak Peek** accellera SYSTEMS INITIATIVE	**Streamlining Low-Power Verification: From UPF to Signoff (continued)** SYNOPSYS	**Your SoC, Your Topology** ARTERIS IP	
17:00 - 18:00	**Welcome Reception** (Bayshore Ballroom)			

DVCon U.S. 2024 - Program Grid
5 March 2024

TIME (PST)	Monterey Carmel	Oak	Fir	Bayshore Ballroom
8:00 - 8:30	**Opening Session** (Oak)			
8:30 - 9:00	**Coffee Break** (Gateway Foyer)			
9:00 - 11:00	**Technical Session #1** (Functional Coverage Closure)	**Technical Session #2** (AI & ML in Verification)	**Technical Session #3** (Formal Verification Use Cases)	
11:00 - 12:30	**Poster Session** (Gateway Foyer)			
12:30 - 13:30	**Lunch Sponsored by** cadence® (Pine Cedar)			
13:30 – 14:30	**Keynote: Addressing the Evolving Landscape of Automotive SoCs** (Oak / Fir)			**Exhibit Hall Open**
14:30 - 15:00	**Coffee Break** (Gateway Foyer)			
15:00 – 17:00	**Technical Session #4** (UVM Testbenches)	**Technical Session #5** (Functional Safety and Verification)	**Technical Session #6** (RISCV Design & Verification)	
17:00 – 18:00	**Reception** (Bayshore Ballroom)			

DVCon U.S. 2024 - Program Grid
6 March 2024

TIME (PST)	Monterey Carmel	Oak	Fir	Bayshore Ballroom
8:00 - 9:00	**Panel: When Will We Be Able to Say, "EDA-GPT, Verify my ASIC"?** (Oak/Fir)			
9:00 - 9:30	**Coffee Break** (Gateway Foyer)			
9:30 – 11:00	**Technical Session #7** (Regression Management Techniques)	**Technical Session #8** (Mixed Signal with UVM Verification)	**Technical Session #9** (SystemVerilog Verification Techniques)	
11:00 – 12:00	**Poster Ninja Warrior** (Oak)			
12:00 – 13:30	**Lunch Sponsored by:** SIEMENS (Pine Cedar)			
13:30 – 14:30	**Keynote: Alex Starr, AMD Corporate Fellow** (Oak / Fir)			
14:30 – 15:00	**Coffee Break** (Gateway Foyer)			
15:00 – 16:30	**Technical Session #10** (Requirements Definition and Traceability)	**Technical Session #11** (Formal: Liveness and Use Cases)	**Technical Session #12** (Analog Modeling in SystemVerilog)	**Exhibit Hall Open**
16:30 – 17:00	**Break**			
17:00 – 17:30	**Best Paper Presentation** (Bayshore Ballroom)			
17:30 – 18:30	**Reception** (Bayshore Ballroom)			

DVCon U.S. 2024 - Program Grid
7 March 2024

TIME (PST)	Cascade	Donner	Siskiyou
9:00 – 10:30	**Data-Driven Design, Verification, Validation, and Signoff Case Studies of RISC-V SoCs** SIEMENS	**Emulation Moves Into 4-State Logic and Real Number Modeling** cadence	**SystemC Model Code Generation using Large Language Models** Vayavya Labs
10:30 – 11:00	**Coffee Break** (Bayshore Foyer)		
11:00 – 12:30	**Data-Driven Design, Verification, Validation, and Signoff Case Studies of RISC-V SoCs (continued)** SIEMENS	**FPGA Prototyping for Large Multi-Die / Multi-Core Designs** SYNOPSYS®	**Advanced UCIe-based Chiplets verification from IP to SoC** cadence
12:30 – 13:30	**Lunch Sponsored by:** SYNOPSYS® (Sierra)		
13:30 – 15:00	**Expanding role of Static Signoff in Verification Coverage** REAL INTENT	**RISC-V Core Verification: A New Normal in Verification Techniques** BREKER™	**Automating the Integration Workflow with IP Centric Design** PERFORCE

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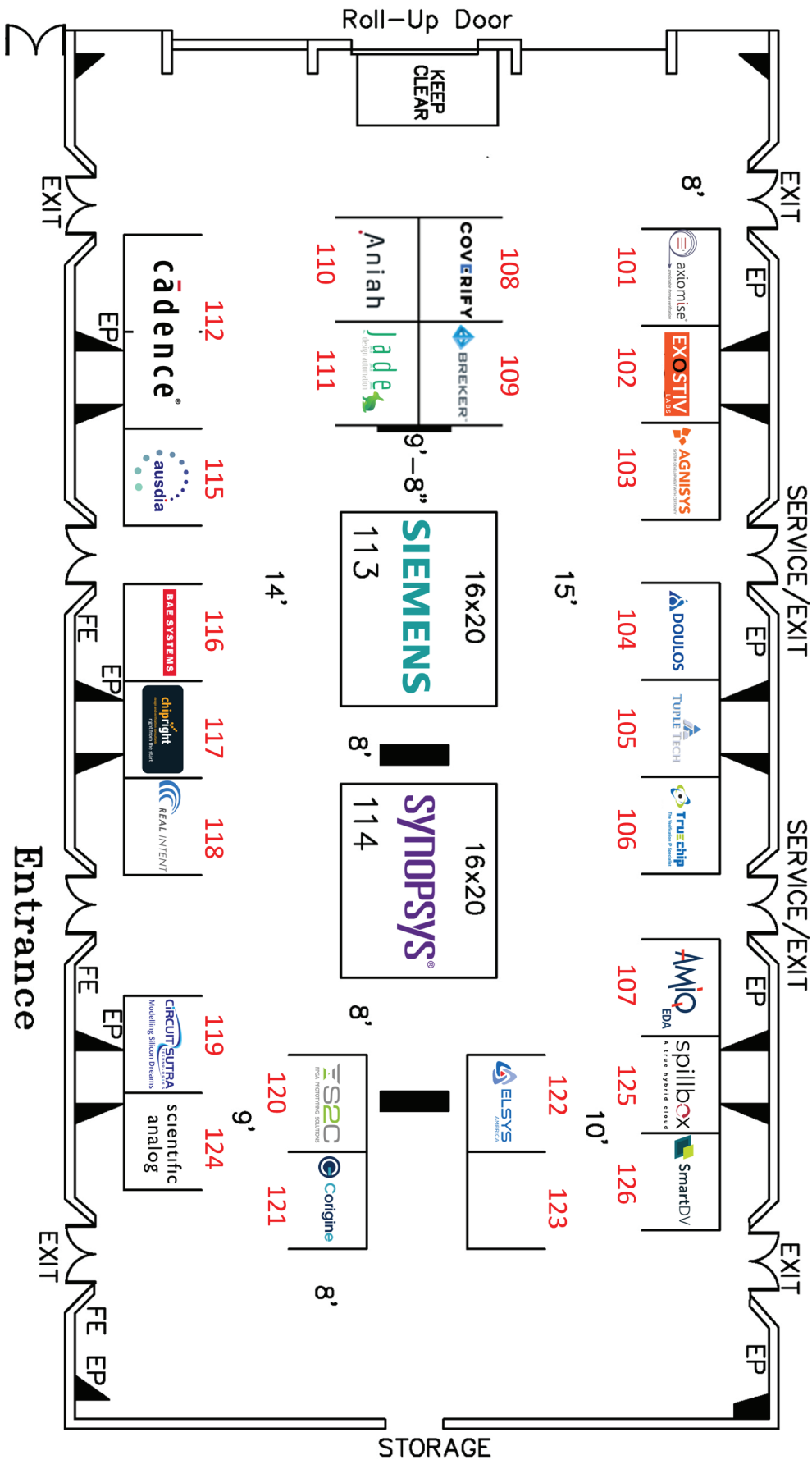
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DVCON U.S. 2024 EXHIBIT HALL MAP



Technical Program: Monday, March 4
Time Zone is PST

9:00–10:30
Tutorial: Portable Stimulus
Room: Monterey Carmel
Presented by members of Accellera System Initiative

Speakers: **Adnan Hamid,** Breker; **Tom Fitzpatrick,** Siemens EDA; **Matthew Ballance,** AMD; **Sergey Khaikin,** Cadence; **Prabhat Gupta,** AMD

Efficient Portable Programming-Sequence Development with PSS

Bringing an SoC-level system out of reset into an operational state involves configuring the component subsystems and IPs by properly programming hundreds or thousands of IP registers. Running behavior involves programming yet more registers and in-memory descriptors. Stake holders, including block-DV, subsystem, SoC verification, silicon bring-up teams, rely on having early access to accurate programming sequences in order to shift-left their activities. Many of these stakeholders also depend on being able to efficiently modify/adjust the programming sequences to exercise different legal configurations and operations.

Current approaches to deriving bring-up sequences often require block-level teams to create some C code that captures key register-programming sequences to hand off to subsystem and SoC teams. Creating this content is an extra task that the block-level team would not normally perform, and is often deferred until late in the verification cycle. This limits the ability of subsystem and SoC teams to left-shift their activities. The programming sequences are typically highly directed, and cannot be easily modified to exercise different scenarios. Finally, because creating C-code programming sequences is disconnected from the primary work of a block-level DV team, they are at high risk of becoming outdated.

This tutorial will also provide an overview of the PSS features in development for PSS 3.0, as well as an introduction to the PSS methodology library currently under development by the working group.

9:00–10:30
Tutorial: USF-based FMEDA-driven Functional Safety Verification
Room: Oak
Presented by Cadence

Speakers: **Francesco Lertora,** Group Director, Software Engineering, Cadence Design Systems, Inc.; **Mangesh Mukundrao Pande,** Solutions Architect, Cadence Design Systems, Inc.; **Pete Hardee, Group Director,** Product Management, Cadence Design Systems, Inc.

Abstract: As the degree of automation continues to increase, the intelligent SoC content in automobiles is growing faster than the general semiconductor market. As a result, the traditional automotive electronics suppliers are being rapidly joined in the market by many other established semiconductor companies and startups, as well as OEMs seeking differentiation through increased vertical integration. This ever-growing set of players all need to meet the functional safety requirements specified in standards such as ISO 26262. A process called Failure Modes, Effects, and Diagnostic Analysis (FMEDA) is critical to meeting these requirements. FMEDA so far has largely been the preserve of consultants using spreadsheet-based approaches. But now, automotive semiconductor design projects are looking for tools offering greater automation and consistency, as well as greater ownership and integration with the design and verification flow, of the FMEDA process. We believe the inherent ambiguity of functional safety standards will finally converge into a consolidated EDA standard to enable automation, results consistency, and information exchange between integrators into a product development lifecycle, analogous to industry standards for hardware description languages, timing, and power constraints.

In this workshop, Cadence will present the Midas™ Safety Platform, and how it uses the Unified Safety Formal (USF) – a formalized method for safety analysis and specification of safety mechanisms proposed as a candidate standard to Accellera's Functional Safety Working Group – to provide a holistic and automated approach to FMEDA at the architectural, design, and diagnostic coverage verification stages. We will demonstrate how USF provides the links between the FMEDA process and digital design and verification flows for both digital and analog/mixed signal, to provide a complete and consistent approach to meeting functional safety requirements.

Technical Program: Monday, March 4 (cont.)

Time Zone is PST

9:00–10:30

Workshop: IP-XACT
Room: Fir
Presented by members of Accellera System Initiative

Speakers: **Richard Weber,** Arteris

Introduction: This tutorial explains basic usage of IP-XACT IEEE 1685-2022 for IP re-use and integration flows.

Summary: This workshop explains the data model underlying the IP-XACT standard. This SoC data model unifies logical and physical connectivity as well as memory map and registers which enables the standard to be used as a single source of truth to automate large parts of SoC front-end design and verification flows.

The workshop will address IP-XACT concepts that are relevant to understand the overall SoC data model such as:

- Components
- Design and Design Configurations
- Bus and Abstraction Definition
- Component Memory Maps and Registers
- Component Address Spaces and Bus Interface Bridges
- Type Definitions

10:30 – 11:00

Coffee Break
Room: Gateway Foyer

11:00 – 12:30

Tutorial: Portable Stimulus (continued)
Room: Monterey Carmel
Presented by members of Accellera System Initiative

Speakers: **Adnan Hamid,** Breker; **Tom Fitzpatrick,** Siemens EDA; **Matthew Ballance,** AMD; **Sergey Khaikin,** Cadence; **Prabhat Gupta,** AMD

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11:00 – 12:30

Tutorial: USF-based FMEDA-driven Functional Safety Verification (continued)
Room: Oak
Presented by Cadence

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11:00 – 12:30

Workshop: Hierarchical CDC and RDC closure with standard abstract models
Room: Fir
Presented by members of Accellera System Initiative

Abstract: As complexity and the number of clock domains increase in today's ASIC designs, we are moving towards a hierarchical verification approach. This tutorial covers the proven clock domain crossings (CDC) and Reset Domain Crossing (RDC) schemes, the verification challenges, and the potential risk mitigation strategies. We will then discuss the hierarchical CDC/RDC verification methodology, the tradeoffs faced when incorporating units from multiple sources, and the challenges when integrating multiple vendor-generated abstracted blocks into an encompassing design. To mitigate these issues, we introduce the Accellera CDC committee, highlight the released CDC standard, and summarize the status of the current efforts.

Topics:

- CDC-RDC Basic Knowledge
- Clock domain crossing schemes
- Reset domain crossing schemes
- CDC-RDC Verification
- Hierarchical CDC Verification
- Accellera CDC Working Group

Speakers:

- Ping Yeung, Nvidia
- Iredamola Olopade, Intel
- Kranthi Pamarthi, Renesas Electronics
- Chetan Choppali Sudarshan, Marvell Technology
- Sean O'Donohue, Synopsys
- Farhad Ahmed, Siemens EDA
- Bill Gascoyne, Blue Pearl
- Anupam Bakshi, Agnisys

Technical Program: Monday, March 4 (cont.)
Time Zone is PST

12:30 – 13:30
Lunch Sponsored by Accellera System Initiative
Room: Pine Cedar

Speakers: **Lu Dai,** Accellera Chair; **Mark Burton,** Principal Engineer, Qualcomm; **Yury Bayda**, Principal Software Engineer, Ford Motor Company

Abstract: Join Accellera for an informative luncheon focused on the efforts and direction of the Federated Simulation Standard Proposed Working Group (FSS PWG). The luncheon will begin with an update on Accellera working group activity from Chair Lu Dai, followed by the presentation of a Distinguished Service Award to a long-time friend of Accellera.

13:30 – 15:00
Workshop: Automatic generation of Device Driver and Programmer's Reference Manual from PSS
Room: Monterey Carmel
Presented by Agnisys

Speakers: **Freddy Nunez,** Applications Engineer, Agnisys Inc.; **Neena Chandawale,** Applications Engineer, Agnisys Inc

Abstract: Embedded systems projects pose significant challenges due to tight schedules and frequent hardware and software redesigns. Creating IP/SoC and their device drivers, especially for diverse components like image sensors and processors, with 10's of 1000's of registers, operating modes and configurations, is time-consuming and error-prone. Informal communication between hardware and software teams further complicates the process, exacerbated by the need for drivers compatible with various operating systems.

To address these challenges, an innovative solution involves automatically generating not just the IP/SOC RTL but also their device driver code. This approach aims to enhance communication between teams by helping them collaborate using the industry standard such as PSS and SystemRDL. The generated sequences support multiple environments, including UVM and C++, reducing the effort required for individual driver development and ensuring compatibility across different environments.

Having a common understanding of the programming sequences not only helps the project move faster towards first pass silicon success but also helps reach the complete system development milestone faster. The Programmer's Reference Manual is a product of this automation which enables the firmware and software teams to deliver the system software earlier in the development process.

13:30 – 15:00
Tutorial: Streamlining Low-Power Verification: From UPF to Signoff
Room: Oak
Presented by Synopsys

Speakers: **Tushar Parikh,** Principal Applications Engineer

Abstract: Generative AI created a lot of interest recently and is poised to change our lives in many unimaginable ways. One significant change we already know is the huge amount of power it consumes: an AI chip with the functionality of GPT-3 and 175 billion parameters would require an estimated 1280 megawatt-hours, which is equivalent to about 120 gasoline-powered cars operating for one year and creating around 550 tons carbon emissions.

Generative AI and other similar applications leverage semiconductor devices, so it is imperative that such devices consume as little power as possible. The most common power saving schemes are clock gating, separating power domains and voltage islands, installing retention cells, and designing efficient power management units.

Tutorial: Streamlining Low-Power Verification: From UPF to Signoff (cont.)

These low-power instruments add circuitry to the design and potentially impact design behavior. Verifying the functional intent of the design in the presence of the low-power constructs is critical. Low-power signoff is a new verification requirement for the chip design and verification community.

Just as functional verification and signoff requires different techniques, such as static, formal, simulation, and hardware prototyping to ensure design integrity, the same is true for functional verification of low-power designs.

This tutorial offers a comprehensive overview of various low-power design techniques as well as the corresponding, recommended verification steps. You will be provided with complete understanding of what it takes for low-power signoff. Topics covered include:

Generation, optimization and maintenance of UPF throughout the flow
Static low-power checks at different stages of the design and verification flow, from UPF creation to gate-level design connected to power-ground (PG) pins
Formal connectivity checking and property verification in the presence of low-power elements in the design, including optimization of clock gating and retention to improve PPA
Dynamic, low-power simulation to further ensure design functionality in the presence of UPF
Debug of issues that arise during low-power verification
You will hear from low-power experts to gain a solid understanding of steps to implement and verify a solid low-power strategy that reduces silicon power consumption. This practical knowledge will prepare you for the trend of ever lower power consuming designs.

13:30 – 15:00

Workshop: Functional Safety
Room: Fir
Presented by Accellera Systems Initiative

The implementation of Functional Safety standards such as ISO26262 poses challenges during the exchange and integration of functional safety data between different work products and activities, carried out by different teams and/or different layers of the supply chain. Automation with EDA tools is now common practice in this field, but interoperability is still challenged by the lack of a Functional Safety standards that supports the data exchange. The Accellera Functional Safety Working Group has recently completed a white paper that describes the approach taken to develop the data model and a corresponding language prototype that will enable Functional Safety data exchange. As a next step, the focus for the Working Group is to develop the LRM (Language Reference Manual) for the Functional Safety Standard. This session will review the content of the white paper and discuss the plans to proceed with the LRM.

15:00 – 15:30

Coffee Break
Room: Gateway Foyer

15:30 – 17:00

Workshop: UVM & A Practical Guide to SA-EDI Methodology
Room: Monterey Carmel
Presented by Accellera Systems Initiative

Speakers: **Jean-Philippe Martin,** Intel; **Mike Borza,** Synopsys

UVM Abstract: The Accellera UVM Working Group released the IEEE 1800.2-2020-2.0 reference library last year. Since that release, we have been working on a public Github repository to give users enhanced access to the latest bug fixes and to provide bug fix suggestions if they would like. Also, we have developed new, additive features to poll an arbitrary DUT signal and to recover appropriately when a process (e.g. a sequence) is terminated abruptly such as by a “disable fork”. In this session, we will provide the details of the new features and explain how

Workshop: UVM & A Practical Guide to SA-EDI Methodology (cont.)

we plan to interact with users via the public repository. There will be generous time for Q&A.

A Practical Guide to SA-EDI methodology Abstract: This workshop will demonstrate how to identify assets in intellectual property (IP) in accordance with Accellera's Security Annotation for Electronic Design Integration (SA-EDI) standard. This guidance is planned to be documented in the IEEE P3164 Asset Identification whitepaper.

The SA-EDI standard relies heavily on the accurate identification of assets within an IP. Any errors, either false positives or negatives, can render the SA-EDI collateral ineffective or non-applicable. Therefore, it's essential not only to identify assets but also to classify them correctly. However, this is not as straightforward as one may think. Contextual information of the IP's integration, such as security requirements, use-cases, surrounding IPs, etc. are often needed in order to properly identify assets. These are typically defined by the integrated circuit (IC) owner and well after the IP has been developed, which is when the SA-EDI collateral needs to be produced.

To address these challenges, the whitepaper introduces a methodical and practical approach that can be applied by IP owners with limited experience in security practices. The methodology is vetted using four example IPs, ranging from simple to complex, to highlight how an IP developer can use to produce accurate SA-EDI collateral for the IC owner to properly consume and apply. Don't miss this opportunity to enhance your knowledge in security.

15:30 – 17:00

Tutorial: Streamlining Low-Power Verification: From UPF to Signoff (continued)

Room: Oak

Presented by Synopsys

Speaker: **Tushar Parikh,** Principal Applications Engineer

Abstract: Generative AI created a lot of interest recently and is poised to change our lives in many unimaginable ways. One significant change we already know is the huge amount of power it consumes: an AI chip with the functionality of GPT-3 and 175 billion parameters would require an estimated 1280 megawatt-hours, which is equivalent to about 120 gasoline-powered cars operating for one year and creating around 550 tons carbon emissions.

Generative AI and other similar applications leverage semiconductor devices, so it is imperative that such devices consume as little power as possible. The most common power saving schemes are clock gating, separating power domains and voltage islands, installing retention cells, and designing efficient power management units.

These low-power instruments add circuitry to the design and potentially impact design behavior. Verifying the functional intent of the design in the presence of the low-power constructs is critical. Low-power signoff is a new verification requirement for the chip design and verification community.

Just as functional verification and signoff requires different techniques, such as static, formal, simulation, and hardware prototyping to ensure design integrity, the same is true for functional verification of low-power designs.

This tutorial offers a comprehensive overview of various low-power design techniques as well as the corresponding, recommended verification steps. You will be provided with complete understanding of what it takes for low-power signoff. Topics covered include:

Generation, optimization and maintenance of UPF throughout the flow
Static low-power checks at different stages of the design and verification flow, from UPF creation to gate-level design connected to power-ground (PG) pins
Formal connectivity checking and property verification in the presence of low-power elements in the design, including optimization of clock gating and retention to improve PPA

Tutorial: Streamlining Low-Power Verification: From UPF to Signoff (continued)
Dynamic, low-power simulation to further ensure design functionality in the presence of UPF
Debug of issues that arise during low-power verification
You will hear from low-power experts to gain a solid understanding of steps to implement and verify a solid low-power strategy that reduces silicon power consumption. This practical knowledge will prepare you for the trend of ever lower power consuming designs.

15:30 – 17:00

Workshop - Your SoC, Your Topology
Room: Fir
Presented by Arteris

Speakers: **Ami Pathak,** Senior Staff Field Application Engineer, Arteris; **Matthew Mangan,** Senior Manager, Corporate Application Engineering, Arteris

Advances in semiconductor process nodes and FinFET transistor design have benefitted System-on-Chip (SoC) technology by allowing more IP to exist on-chip. The increased amount of on-chip IP results in more complex on-chip interconnect requirements to handle the communication between all the IP blocks. Consequently, the interconnect has become a prime source of SoC design challenges in both frontend and backend flows.

Traditional interconnect IP offerings tend to box users into a fixed switch topology, most commonly a cascaded crossbar, forcing SoC teams to design around the interconnect IP's limitations in ways that magnify challenges rather than solve them. In this tutorial, we will explore how Network-on-Chip (NoC) interconnect IP address the problem of on-chip communication differently than traditional interconnects and enable SoC teams to create a topology that is optimized for their SoC requirements. We will also introduce a framework for how SoC teams can approach NoC topology optimization in their projects.

Attendees will come away with:

- Differences between NoCs and traditional interconnects
- Tradeoffs between different interconnect topologies
- How to approach finding an optimal interconnect topology for a given set of performance and physical requirements

17:00 – 18:00

Welcome Reception
Room: Bayshore Ballroom

Technical Program: Tuesday, March 5
Time Zone is PST

8:00 – 8:30

Opening Session
Room: Oak

8:30 – 9:00

Coffee Break
Room: Gateway Foyer

9:00 – 11:00

Technical Session #1 (Functional Coverage Closure)
Room: Monterey Carmel
Session Chair: **Srivatsa Vasudevan**

[1021] Functional Coverage Closure with Python
Seokho Lee, FuriosaAI; **Youngsik Kim,** FuriosaAI; **Suhyung Kim,** FuriosaAI; **Jeong Ki Lee,** FuriosaAI; **Wooyoung Choe,** FuriosaAI; **Minho Kim,** FuriosaAI

[1074] Automated Generation of Interval Properties From Trace-Based Function Models
Robert Kunzelmann, Infineon Technologies AG, Technical University of Munich; **Aishwarya Sridhar,** Infineon Technologies AG; **Daniel Gerl,** Infineon Technologies AG, Technical University of Munich; **Lakshmi Vidhath Boga,** Infineon Technologies AG; **Wolfgang Ecker,** Infineon Technologies AG, Technical University of Munich

[1062] Tackling Missing Bins: Refining Functional Coverage in SystemVerilog for Deterministic Coverage Closure
Jikjoo Lee, Samsung Electronics, Memory Division South Korea; **Kihyun Park,** Samsung Electronics, Memory Division South Korea; **Tony Gladvin George,** Samsung Electronics, Memory Division South Korea; **Dongkun An,** Samsung Electronics, Memory Division South Korea; **Wooseong Cheong,** Samsung Electronics, Memory Division South Korea; **Byungchul Yoo,** Samsung Electronics, Memory Division South Korea

[1090] mL: Shrinking the Verification volume using Machine Learning
Yash Phogat, Arm Inc.; **Patrick Hamilton,** Arm Inc.

Technical Program: Tuesday, March 5
Time Zone is PST

9:00 – 11:00

Technical Session #2 (AI & ML in Verification)
Room: Oak
Session Chair: **Harry Foster**

[1044] Requirements Recognition For Verification Ip Design Using Large Language Models
Siarhei Zalivaka, Solidigm

[1083] All Artificial, Less Intelligence: GenAI through the Lens of Formal Verification
Aman Kumar, Infineon Technologies; **Deepak Narayan Gadde,** Infineon Technologies; **Thomas Nalapat,** Infineon Technologies; **Evgenii Rezunov,** Infineon Technologies; **Fabio Cappellini,** Infineon Technologies

[1104] Efficient application of AI algorithms for large-scale verification environments based on NoC architecture
Olivera Stojanovic, Vtool; **Nemanja Mitrovic,** Vtool; **Anna Revitzki,** Vtool

[1135] Large Language Model for Verification: A Review and Its Application in Data Augmentation
Dan Yu, Siemens EDA; **Harry Foster,** Siemens EDA; **Eman El Mandouh,** Siemens EDA; **Waseem Raslan,** Siemens EDA; **Tom Fitzpatrick,** Siemens EDA

9:00 – 11:00

Technical Session #3 (Formal Verification Use Cases)
Room: Fir
Session Chair: **Erik Seligman**

[1025] Automating the Formal Verification of Firmware: A Novel Foundation and Scalable Methodology
Bryan Olmos, Infineon Technologies AG; **Sanjana Sainath,** Infineon Technologies AG; **Wolfgang Kunz,** Rheinland-PfÃ¤lzische Technische UniversitÃ¤t Kaiserslautern-Landau; **Djones Lettnin,** Infineon Technologies AG

[1027] Automated Formal Verification of a Highly-Configurable Register Generator
Shuhang Zhang, Infineon Technologies AG; **Bryan Olmos,** Infineon Technologies AG; **Basavaraj Naik,** Infineon Technologies AG

[1101] Formal Verification Approach to Verifying Stream Decoders: Methodology & Findings
Abhishek Asi, Intel; **Anshul Jain,** Intel; Virginia Bao, Intel

[1138] New Innovative Way to Verify Packaging Connectivity
Mike Walsh, Siemens EDA; Jin Hou, Siemens EDA

11:00 – 12:30

Poster Session
Room: Gateway Foyer

[1019] RTL Transformation Methods to Achieve Order of Magnitude TAT Improvement in VLSI Design
Ashfaq Khan, Intel Corporation; **Shuhui Lin,** Intel Corporation; **Daniel Standring,** Intel Corporation; **Adam Campos,** Intel Corporation; **Satish Venkatesan,** Intel Corporation; **Soowan Suh,** Intel Corporation

[1020] Arithmetic Overflow Verification using Formal LINT Tools
Kaiwen Chin, Renesas; Esra Sahin, Renesas; **Kranthi Pamarthi,** Renesas

[1024] Innovative 4-State Logic Emulation for Power-aware Verification
Kyoungmin Park, Samsung Electronics; **Brad Budlong,** Cadence Design Systems; **Hyundon Kim,** Samsung Electronics; **Danny Yi,** Cadence Design Systems; **Gibs Lee,** Cadence Design Systems; **Jaehunn Lee,** Samsung Electronics; **Chulmin Kim,** Samsung Electronics; **Jaemin Choi,** Samsung Electronics; **Kijung Yoo,** Samsung Electronics; **Youngsik Kim,** Samsung Electronics; **Yogesh Goel,** Cadence Design Systems; **Seonil Brian Choi,** Samsung Electronics

[1029] A Statistical and Model-Driven Approach for Comprehensive Fault Propagation Analysis of RISC-V Variants
Endri Kaja, Infineon Technologies AG; **Nicolas Gerlin,** Infineon Technologies AG; **Ungsang Yun,** Infineon Technologies AG; **Jad Al Halabi,** Infineon Technologies AG; **Sebastian Prebeck,** Infineon Technologies AG; **Dominik Stoffel,** Rheinland-PfÃ¤lzische Technische UniversitÃ¤t; **Wolfgang Kunz,** Rheinland-PfÃ¤lzische Technische UniversitÃ¤t; **Wolfgang Ecker,** Infineon Technologies AG

[1054] The beginning of new norm: CDC/RDC constraints signoff through functional simulation
Suhas D S, Intel; **Ponsankar Arumugam,** Intel; **Deepmala Sachan,** Intel; **Ritesh Jain,** Intel

[1061] Metric Driven Microcode Verification: Navigating Microcode Coverage Complexities
Seungyeon Yu, Samsung Electronics, Memory Division; **Damin Son,** Samsung Electronics, Memory Division

[1063] Synthetic Traffic based SOC Performance Verification Methodology
Jeonggu Lee, Samsung Electronics Co., LTD.; Taewon Park, Samsung Electronics Co., LTD.; **Hyungtae Park,** Samsung Electronics Co., LTD.; **Taeyoung Jeon,** Samsung Electronics Co., LTD.; **Hyunjae Woo,** Samsung Electronics Co., LTD.; **Youngsik Kim,** Samsung Electronics Co., LTD.; **Seonil Brian Choi,** Samsung Electronics Co., LTD.

[1065] Shift Left on Timing Constraints Verification: Beyond Typical Front-End Execution
Vineeth B, Intel Technology India Pvt Ltd; **Deepmala Sachan,** Intel Technology India Pvt Ltd; **Ritesh Jain,** Intel Technology India Pvt Ltd

[1088] On Analysis of RDC issues for identifying Reset tree design bugs and further strategies for Noise Reduction
Farhad Ahmed, Siemens EDA; **Manish Bhati,** Siemens EDA; Lyle Benson, Siemens EDA

[1102] Interoperability Validation Without Direct Integration
Nicholas Nuti, Intel Corporation; **Srinivasan Jambulingam,** Intel Corporation

[1117] AI-based Algorithms to Analyze and Optimize Performance Verification Efforts
Sharada Vajja, Google LLC; **Raghu Alamuri,** Google LLC; Saksham Mehra, Google LLC

[1124] Achieving End-to-End Formal Verification of Large Floating-Point Dot Product Accumulate Systolic Units
Emiliano Morini, Intel; **Bill Zorn,** Intel; **Disha Puri,** Intel; **Madhurima Eranki,** Intel; **Shravya Jampana,** Intel

[1131] Towards Efficient Design Verification – Constrained Random Verification using PyUVM
Deepak Narayan Gadde, Infineon Technologies; **Suruchi Kumari,** Infineon Technologies; **Aman Kumar,** Infineon Technologies

[1140] Enabling True System-Level, Mixed-Signal Emulation
Nimay Shah, Analog Devices Inc.; **Pranav Dhayagude,** Analog Devices Inc.; **Paul Wright**, Analog Devices Inc.; **Raj Mitra,** Cadence Design Systems Inc.

Technical Program: Tuesday, March 5 (cont.)
Time Zone is PST

11:00 – 12:30

Poster Session (cont.)

[1141] A UVM SystemVerilog Testbench for Directed and Random Testing of an AMS Low-Dropout Voltage Regulator
Charles Dancak, Betasoft Inc.

[1145] Scalable Functional Verification using Portable Stimulus Standard
Santosh Kumar, Qualcomm Technologies Inc; **Yogish Raja,** Qualcomm Technologies Inc; **Geetika Agrawal,** Qualcomm Technologies Inc; **Karthikeyan Sugumaran,** Qualcomm Technologies Inc; **Arjun Vazhayil,** Qualcomm Technologies Inc; **Tommy Brunansky,** Qualcomm Technologies Inc.

12:30 – 13:30

Lunch Sponsored by Cadence
Room: Pine Cedar

Speaker: **Moshe Y. Vardi,** Rice University

How to be an ethical technologist

Many of us got involved in computing because programming was fun. The advantages of computing seemed intuitive to us. We truly believed that computing yields tremendous societal benefits; for example, the life-saving potential of driverless cars is enormous! Recently, however, many technologists realized that computing is not a game--it is real--and it brings with it not only societal benefits, but also significant societal costs, such as labor polarization, disinformation, smart-phone addiction, and more.

A common reaction to this crisis is to label it as an "ethics crisis".

But corporations are driven by profits, not ethics, and machines are just machines. Only people can be expected to act ethically. In this talk the speaker will discuss how technologists should behave ethically.

13:30 – 14:30

Keynote: Addressing the Evolving Landscape of Automotive SoCs
Room: Oak / Fir
Paul Cunningham, Cadence Design Systems; **Anthony Hill,** Texas Instruments Fellow

Automotive and industrial SOCs have extremely high design and verification complexities. These devices integrate a broad range of IP – simple sensors, complex interface IP (e.g., DDR), accelerators (e.g., GPU/AI), industrial interface IP (e.g., CAN), safety and security (e.g., tamper), etc. These IP can come from widely dissimilar sources – often internal as well as multiple external ("third-party") sources. These SOCs typically support a wide range of customer use cases and software stacks. After a brief introduction to this problem and scope, we will cover two major topics. First, we will look at some case study silicon escapes, root cause, and potential corrective actions. Second, we will look at evolving requirements in this space and the impact to design verification scope.

Technical Program: Tuesday, March 5 (cont.)
Time Zone is PST

14:30 – 15:00

Coffee Break
Room: Gateway Foyer

15:00 – 17:00

Technical Session #4 (UVM Testbenches)
Room: Monterey Carmel
Session Chair: **Peter George**

[1031] Leveraging Model Based Verification for Automotive SoC
Aswini Kumar Tata, ALLEGRO MICROSYSTEMS LLC; **Bhanu Singh,** MathWorks; **Sanjay Chatterjee,** ALLEGRO MICROSYSTEMS LLC; **Eric Cigan,** MathWorks; **Surekha Kollepara,** ALLEGRO MICROSYSTEMS LLC; **Kamel Belhous,** Allegro Microsystems

[1047] A UVM Multi-Agent Verification IP architecture to enable Next-Gen protocols with enhanced reusability, controllability and observability
Prathik R, Samsung Semiconductor India Research, Bengaluru; **Ramesh Madatha,** Samsung Semiconductor India Research, Bengaluru; **Girish Kumar Gupta,** Samsung Semiconductor India Research, Bengaluru; **Tony Gladvin George,** Samsung Electronics, Korea

[1103] Leveraging Interface Classes to Improve UVM TLM
Neha Goyal, Nvidia Corp.; **Justin Refice,** Nvidia Corp.

[1116] Without Objection - Touring the uvm_objection implementation - uses and improvements
Rich Edelman, Siemens EDA

15:00 – 17:00

Technical Session #5 (Functional Safety and Verification)
Room: Oak
Session Chair: **Jamie Ridgeway**

[1022] Leveraging Several Functional Safety Methodologies (Full Faults and SRF) to Enhance Design Quality in Automotive IC
Sougata Bhattacharjee, Samsung Semiconductor India Research (SSIR); **Gulshan Kumar Sharma,** Samsung Semiconductor India Research (SSIR); **Wonil Cho,** Samsung Electronics; **Akshaya Kumar Jain,** Samsung Semiconductor India Research (SSIR); **James Kim,** Siemens; **Andrey Likhopoy,** Samsung Electronics; **Sangkyu Park,** Samsung Electronics; **Hyeonuk Noh,** Samsung Electronics; **Ann Keffer,** Siemens; **Arun Gogineni,** Siemens

[1040] Functional Safety Workflow of Internal IP (NPU) Within Large Automotive IC Through Analysis and Emulation Usage for SW-based Safety Mechanisms
Andrey Likhopoy, Samsung Electronics; **Sangkyu Park,** Samsung Electronics; **Hyeonuk Noh,** Samsung Electronics; **Wonil Cho,** Samsung Electronics; **Inhwan Kim,** Siemens EDA; **Robert Serphillips,** Siemens EDA; **Chanjin Kim,** Siemens EDA; **Justin Lee,** Siemens EDA; **James Kim,** Siemens EDA; **Sougata Bhattacharjee,** Samsung Semiconductor India Research (SSIR); **Gulshan Kumar Sharma,** Samsung Semiconductor India Research (SSIR); **Akshaya Kumar Jain,** Samsung Semiconductor India Research (SSIR)

[1052] AI based Media Functional safety and Reliability verification in Safety-Critical Autonomous Systems
Suresh Vasu, Intel Corporation; **palanivel guruvareddiar,** Intel Corporation; **Pooja Sundar,** Intel Corporation

[1068] Are My Fault Campaigns Providing Accurate Results for Iso 26262 Certification?
James(JAE YUN) Kim, Siemens EDA; **Arun Gogineni,** Siemens EDA; **Ann keffer,** Siemens EDA; **Ahn Hyunsun,** Samsung LSI

Technical Program: Tuesday, March 5 (cont.)

Time Zone is PST

15:00 – 17:00

Technical Session #6 (RISCV Design & Verification)
Room: Fir
Session Chair: **Kamel Belhous**

[1008] Crafting a Million Instr/Sec RISCV-DV -- HPC Techniques to Boost UVM Testbench Performance by over 100x
Puneet Goel, Incore Semiconductors; **Ritu Goel,** Coverify Systems Technology; **Jyoti Dahiya,** Coverify Systems Technology

[1081] RISC-V Testing – status and current state of the art
Jon Taylor, Imperas Software

[1055] Unleashing the Power of Whisper for block-level verification in high performance RISC-V CPU
Chenhui Huang, Tenstorrent Inc.; **Yu Sun,** Tenstorrent Inc.; J**oe Rahmeh,** Tenstorrent Inc.

[1136] Extending the RISC-V Verification Interface for Debug Module Co-simulation
Aimee Sutton, Imperas Software Ltd.

17:00 - 18:00

Reception
Room: Bayshore Ballroom

Technical Program: Wednesday, March 6
Time Zone is PST

8:00 – 9:00

Panel: When Will We Be Able to Say, "EDA-GPT, Verify my ASIC"?
Room: Oak / Fir
Abstract: Goldman Sachs estimates that up to 25% of jobs in the US and a staggering 300 million jobs globally will be affected by generative AI. As contributors to the semiconductor industry, we find ourselves both accelerating and being impacted by this transformative trend. While AI and machine learning have already made strides in verification, the advent of Generative AI, particularly Large Language Models (LLMs), introduces fresh possibilities for enhancing verification productivity through acceleration, automation, and heightened accuracy. However, the critical question remains – can these promises materialize?

Many verification teams have either integrated LLMs into their daily workflows or are in the planning stages to do so. Simultaneously, concerns linger around data privacy, potential job displacement, and role changes. This panel invites participants to share and discuss their perspectives, experiences, insights, and apprehensions regarding the role of generative AI in verification. By doing so, the panel aims to offer the audience a glimpse into the future of verification, driven by LLMs, which is rapidly approaching.

Panel Participants:

Moderator:

Harry Foster, Chief Scientist Verification, Siemens EDA

Panelists:

Erik Berg, Principal SoC Verification Engineer, Microsoft

Daniel Schostak, Verification Architect & Fellow, ARM

Mark Ren, Director of Design and Automation Research, NVIDIA

Dan Yu, AI/ML Solutions Manager, Siemens EDA

9:00 – 9:30

Coffee Break
Room: Gateway Foyer

9:30 – 11:00

Technical Session #7 (Regression Management Techniques)
Room: Monterey Carmel
Session Chair: **Progyna Khondkar**

[1078] Bus Trace System: Automated Bus Traffic Debugging in IP-XACT Based SoC Beyond Traditional Debugging Methods
So Wonyeong, Samsung Electronics; **Yang Yonghyun,** Samsung Electronics; **Roe Sun-il,** Samsung Electronics; **Jang Moonki,** Samsung Electronics; **Kim Youngsik,** Samsung Electronics; **Choi Seonil,** Samsung Electronics

[1095] Functional Verification from Chaos to Order: Using Continuous Integration for Hardware Functional Verification
Kirolos Mikhael, Siemens EDA; **Abelouhab Ayari,** Siemens EDA

[1099] Novel Method To Speed-Up UVM Testbench Development
Prashantkumar Ravindra, Analog Devices; **Barry Briscoe,** Analog Devices; **Miguel Castillo,** Analog Devices; **Nimay Shah,** Analog Devices

Technical Program: Wednesday, March 6
Time Zone is PST

9:30 – 11:00

Technical Session #8 (Mixed Signal with UVM Verification)
Room: Oak
Session Chair: **Greg Tumbush**

[1112] Advanced UVM Based Chip Verification Methodologies with Full Analog Functionality
Simul Barua, Ulkasemi Inc.; FNU Farshad, Ulkasemi Inc.; **Henry Chang,** Designerâ€™s Guide Consulting, Inc.

[1137] UVM Testbench Automation for AMS Designs
Jonathan David, Innophase, Inc.; **Henry Chang,** Designer's Guide Consulting, Inc.

[1160] DV UVM based AMS co-simulation and verification methodology for mixed signal designs
Sandeep Sharma, Meta platforms Inc.

9:30 – 11:00

Technical Session #9 (SystemVerilog Verification Techniques)
Room: Fir
Session Chair: **Dave Rich**

[1035] Practical Asynchronous SystemVerilog Assertions
Doug Smith, Doulos

[1087] Working within the Parameters that SystemVerilog has constrained us to
Salman Tanvir, Infineon Technologies; **David Crutchfield,** Infineon Technologies; **Markus Brosch,** Infineon Technologies

[1134] Four Problems with Policy-Based Constraints and How to Fix Them
Dillan Mills, Synopsys, Inc.; **Chip Haldane,** The Chip Abides, LLC

11:00 – 12:00

Poster Ninja Warrior
Room: Oak

12:00 – 13:30

SIEMENS

Lunch Sponsored by Siemens
Room: Pine Cedar
How Your D-V Challenges Drive Our Innovation: Insights from the Top

Companies in the semiconductor and systems industry are in a new, transformative design and verification cycle; driven by trends like the move from monolithic SoCs to chiplets, AI/ML and specialized accelerators, and end-product specific applications. There are very few markets that are immune to these transformational dynamics. And as the pace of change in design and verification continues to break current flows, the demands for new innovative tools, flows, and methodologies to support those changes increases exponentially.

In this discussion, Ron Wilson, industry veteran, invites the panelists to address the challenges of transformation in the design, verification, and validation landscape, and provide insight into what lies ahead in 2024.

Technical Program: Wednesday, March 6 (cont.)

Time Zone is PST

13:30 – 14:30

Keynote: From Chips to Checkered Flags: The Race Towards Real World Innovation
Room: Oak / Fir
Alex Starr, AMD Corporate Fellow

14:30 – 15:00

Coffee Break
Room: Gateway Foyer

15:00 – 16:30

Technical Session #10 (Requirements Definition and Traceability)
Room: Monterey Carmel
Session Chair: **Paul Marriott**

[1002] PyRDV: a Python-based solution to the requirements traceability problem
Fernando Orge, Allegro MicroSystems

[1009] Verification Plan in Requirements Management Tool: Simple Traceability and Automated Interface to Regression Manager
Jan Kreisinger, Allegro MicroSystems, Inc; **Sanjay Chatterjee,** Allegro MicroSystems, Inc

[1133] Gherkin Implementation in SystemVerilog Brings Agile Behavior-Driven Development to UVM
William Moore, Paradigm Works

15:00 – 16:30

Technical Session #11 (Formal: Liveness and Use Cases)
Room: Oak
Session Chair: **Xiaolin Chen**

[1016] Forward Progress checks in Formal Verification: Liveness vs Safety
Ankit Garg, Nvidia

[1114] Liveness Assume-Guarantee Proof Schema: A step towards Liveness Full Proofs
Nitish Sharma, Qualcomm Inc; **Venkata Nishanth Narisetty,** Qualcomm Inc

[1036] Next-Generation Formal Property Verification: Lightweight Theorem Proving Integrated into Model Checking
Erik Seligman, Cadence; **Karthik Baddam,** Qualcomm

Technical Program: Wednesday, March 6 (cont.)
Time Zone is PST

15:00 – 16:30

Technical Session #12 (Analog Modeling in SystemVerilog)
Room: Fir
Session Chair: **Shekar Chetput**

[1049] Functional Verification of Analog Devices modeled using SV-RNM
Mariam Maurice, Siemens EDA

[1091] Variation-aware modeling method for MRAM behavior model using System-Verilog
SangGi Do, Samsung Electronics; **Seongeun Shin,** Samsung Electronics; **JungKyu Jang,** Samsung Electronics; **Dohui Kim,** Samsung Electronics

[1156] SV_LUT: A SystemVerilog Look Up Table package for developing complex AMS Real Number Modeling
FNU Farshad, Ulkasemi Inc; **Shafaitul Islam Surush,** Ulkasemi Inc.; **Simul Barua,** Ulkasemi Inc

16:30 – 17:00

Break

17:00 – 17:30

Best Paper Presentation
Room: Bayshore Ballroom

17:30 – 18:30

Reception
Room: Bayshore Ballroom

9:00 – 10:30

Tutorial: Data-Driven Design, Verification, Validation, and Signoff Case Studies of RISC-V SoCs

Room: Cascade

Presented by Siemens EDA

SIEMENS

Abstract: Efficiently delivering a first-time right RISC-V-based SoC requires a flow that supports every phase of the development process -- from rigorously validating the RTL with simulation and formal methods, to full SoC testing with real world workloads, to specialized C++ or SystemC high-level verification of specialized accelerator IP blocks.

And all of this must come together seamlessly so that the project team has data-driven accountability of their verification coverage and completeness at all times.

In this tutorial, using different open-source RISC-V cores and accelerators for context, we will take you on a detailed journey covering three primary areas:

High-Level Synthesis (HLS) design and verification: Specialized accelerators are commonly incorporated in RISC-V SoCs in the form of new instructions, co-processors, or bus-based accelerators used to off-load compute intensive software functions into hardware. In this segment, we will show how a HLS D&V flow enables designers to rapidly create and evaluate implementation alternatives to achieve the optimal performance, power, and area (PPA) for their design. HLS with C++ or SystemC delivers both an abstract and a low-level VHDL or Verilog RTL model that can be used in downstream verification phases. Our HLS flow has pre-synthesis design checks to find programming errors, verification coverage, and synthesis issues early, as well as both formal and dynamic simulation to verify correctness between the original algorithm and the synthesized RTL.

RTL-level design & verification: In this segment we will cover the elements of RTL D&V flows that RISC-V projects often call for above-and-beyond legacy SoCs: scalable, exhaustive verification of custom processor instructions and other novel logic, validating the root of trust and overall security of the RTL design, and verifying the correct integration of peripherals via standard interfaces (e.g. AMBA, PCIe, UCIe, et.al.) We will also demonstrate how recent advances in static formal verification and dynamic simulation technologies can deliver step-function gains in total user productivity.

Full SoC verification: In this segment of the tutorial, we will explore the complexities of verifying and validating SoCs with real-world stimulus and real workloads. We will show how the Veloce ecosystem provides hardware, software, and systems engineers alike the tools and methodologies to not only shift-left their software development efforts, but also provide visibility and correlation to power profiles, performance, and HW debug. We will discuss the details of what the Veloce Hardware Assisted verification execution platform has in providing a congruent verification experience. Specifically, we will share how to apply the mix of virtual prototype capabilities, hardware emulation and enterprise prototyping technologies, enhanced by easy-to-use apps and solutions, to address challenges common to RISC-V SoCs

Working knowledge of Verilog, SystemVerilog, VHDL, and the principles of code and functional coverage will be assumed.

Instructors:

Russ Klein – HLS design and verification

Andy Meier – Hardware-assisted verification

Erik Jessen – RTL design and verification

John Hallman – Trust and Assurance verification

9:00 – 10:30

Workshop: Emulation Moves Into 4-State Logic and Real Number Modeling

Room: Donner

Presented by Cadence

Speakers: **Brad Budlong,** Cadence Design Systems; **Michael Young,** Cadence Design Systems

Abstract: Since the inception of hardware emulation, emulators have supported verification of digital designs using 2-state logic. The underlying hardware used for emulation has directly modeled the logic of a design with just 0 and 1 values. This workshop will show how support for 4-state logic improves emulation of digital designs and support for real numbers improves emulation for digital mixed signal designs.

4-state logic emulation has a range of applications. Low power verification controlled with UPF is only partially modeled when constrained to 2-state. Here we'll present how the corruption, isolation, and propagation of X values in emulation leads to greater verification and simplified debugging. We'll also look at how introducing the fourth state value Z into emulation improves the verification of multi-driven busses.

All large digital designs must be emulated, but those designs are typically surrounded by analog content for communication to memories, high speed interfaces and RF communication. This analog content is also configured and controlled by processors in the digital design, but the analog content couldn't be emulated. This workshop will show how adding dedicated floating-point hardware to an emulation processor along with extending the emulation software to understand real number handling and the timing constraints of an analog design extends emulation into the mixed signal domain.

9:00 – 10:30

Workshop: SystemC Model Code Generation using Large Language Models

Room: Siskiyou

Presented by Vayavya Labs

Speakers: **Shravan Belagalmath,** Vayavya Labs Pvt. Ltd.; **Sandeep Pendharkar,** Vayavya Labs Pvt. Ltd.; **Karthick Gururaj,** Vayavya Labs Pvt. Ltd.; **Selvin Deva Santhosh Michael,** Vayavya Labs Pvt. Ltd.

OBJECTIVE: This presentation and workshop will cover the challenges and effective approaches to generate SystemC model code for hardware IP peripherals using Large Language Models (LLM). The workshop will show a live demo of LLM model in operation, generating SystemC model of a peripheral device.

INTRODUCTION: With recent developments in AI, Large Language Models are used as assistants to perform various tasks. As these models accept and generate natural language text, they are helpful in various tasks that involves Natural Language Processing like text classification, document summarization, question answering, language translation, chatbots, code generation. Of relevance here is on-going active research and exploration in code generation capability of LLMs to enhance productivity of software developers. The presenters will show application of the same for creating SystemC Transaction Level Model from a high-level input specification.

This abstract is organized into following sections:

- Challenges, this section will mention the challenges faced by in using LLM for SystemC code generation.
- Approach, this section will discuss about approaches that improved code generation results.
- Results, this section will provide analysis of the output generated by OpenAI's GPT – the LLM that was used in this project
- Future work, this section will provide information about features of final product.

Technical Program: Thursday, March 7 (cont.)

Time Zone is PST

10:30 – 11:00

Coffee Break

Room: Bayshore Foyer

11:00 – 12:30

Tutorial: Data-Driven Design, Verification, Validation, and Signoff Case Studies of RISC-V SoCs (cont.)

Room: Cascade

Presented by Siemens EDA

SIEMENS

Abstract: Efficiently delivering a first-time right RISC-V-based SoC requires a flow that supports every phase of the development process -- from rigorously validating the RTL with simulation and formal methods, to full SoC testing with real world workloads, to specialized C++ or SystemC high-level verification of specialized accelerator IP blocks.

And all of this must come together seamlessly so that the project team has data-driven accountability of their verification coverage and completeness at all times.

In this tutorial, using different open-source RISC-V cores and accelerators for context, we will take you on a detailed journey covering three primary areas:

High-Level Synthesis (HLS) design and verification: Specialized accelerators are commonly incorporated in RISC-V SoCs in the form of new instructions, co-processors, or bus-based accelerators used to off-load compute intensive software functions into hardware. In this segment, we will show how a HLS D&V flow enables designers to rapidly create and evaluate implementation alternatives to achieve the optimal performance, power, and area (PPA) for their design. HLS with C++ or SystemC delivers both an abstract and a low-level VHDL or Verilog RTL model that can be used in downstream verification phases. Our HLS flow has pre-synthesis design checks to find programming errors, verification coverage, and synthesis issues early, as well as both formal and dynamic simulation to verify correctness between the original algorithm and the synthesized RTL.

RTL-level design & verification: In this segment we will cover the elements of RTL D&V flows that RISC-V projects often call for above-and-beyond legacy SoCs: scalable, exhaustive verification of custom processor instructions and other novel logic, validating the root of trust and overall security of the RTL design, and verifying the correct integration of peripherals via standard interfaces (e.g. AMBA, PCIe, UCIe, et.al.) We will also demonstrate how recent advances in static formal verification and dynamic simulation technologies can deliver step-function gains in total user productivity.

Full SoC verification: In this segment of the tutorial, we will explore the complexities of verifying and validating SoCs with real-world stimulus and real workloads. We will show how the Veloce ecosystem provides hardware, software, and systems engineers alike the tools and methodologies to not only shift-left their software development efforts, but also provide visibility and correlation to power profiles, performance, and HW debug. We will discuss the details of what the Veloce Hardware Assisted verification execution platform has in providing a congruent verification experience. Specifically, we will share how to apply the mix of virtual prototype capabilities, hardware emulation and enterprise prototyping technologies, enhanced by easy-to-use apps and solutions, to address challenges common to RISC-V SoCs

Working knowledge of Verilog, SystemVerilog, VHDL, and the principles of code and functional coverage will be assumed.

Instructors:

Russ Klein – HLS design and verification

Andy Meier – Hardware-assisted verification

Erik Jessen – RTL design and verification

John Hallman – Trust and Assurance verification

11:00 – 12:30

Workshop: FPGA Prototyping for Large Multi-Die / Multi-Core Designs

Room: Donner

Presented by Synopsys

Speakers: **Joe Marceno,** Synopsys; **Sivaramlingam Palaniappan,** Synopsys

Abstract: Today's design size and complexity continue to increase putting greater pressure on meeting compile time and performance goals of the prototype. Together, they are increasing faster than the available compute capability. This has lead to more challenging implementation problems and longer, unpredictable bring-up times for prototypes. To decouple design sizes and compute capacity, a divide-and-conquer approach is needed. This approach helps to enable parallelism.

This workshop will present enhanced capabilities in Synopsys HAPS ProtoCompiler that can enable parallelism - allowing different teams to solve implementation challenges independently and concurrently. In addition, we will discuss how parallelism enables reuse of such implementations for design types involving multi-cores which are often replicated, ultimately reducing peak compute requirements and leading to faster tool execution times. This modular design approach is a framework that will address these needs while also providing a path to faster incremental TaT.

11:00 – 12:30

Workshop: Advanced UCIe-based Chiplets verification from IP to SoC

Room: Siskiyou

Presented by Cadence

Speakers: **Moshik Rubin,** Sr Product Management Group Director, Cadence; **Anunay Bajaj,** Sr Principal Product Engineer, Cadence

Abstract: The emergence of the Universal Chiplet Interconnect Express (UCIe) standard has revolutionized the electronics industry by enabling the integration of chiplets with diverse functionalities and technology nodes into complex electronic chips. This advancement has introduced new challenges in RTL (Register- Transfer Level) design, particularly in managing protocols like PCIe, CXL, and Streaming, as well as implementing a novel Physical Layer and intricate Die-to-Die adapters. Consequently, the verification complexities of such designs have grown exponentially.

This workshop delves into effective strategies for optimizing verification efforts and enhancing productivity when working with UCIe-based designs, spanning from individual blocks to system-level verification. Attendees will gain practical experience in:

Seamlessly integrating various UCIe blocks with a Device Under Test (DUT).

Streamlining the transition from Intellectual Property (IP) to System-on-Chip (SoC) level.

Measuring and analyzing UCIE based system performance.

Debugging UCIe related scenarios using advanced tools and methods.

Join us in this workshop to uncover solutions for tackling the challenges posed by UCIe-based designs, identifying critical bottlenecks, and visualizing the performance impact, ultimately empowering engineers to create more sophisticated electronic chips efficiently.

12:30 – 13:30

Lunch Sponsored by Synopsys
Room: Sierra

Companies are rapidly adopting multi-die systems to scale functionality, power and performance beyond Moore's law. Multi-die systems are moving innovation forward at a rapid pace, powering significant advances in high-performance computing, AI, mobile, and automotive application.

However, despite the clear advantages, designing a multi-die system versus a traditional monolithic SoC is not easy since design requirements and considerations must be managed at the system level across several heterogeneous dies. There are numerous verification challenges that stand in the way of multi-die system realization, including:

Addressing capacity and performance for system verification

Validating assumptions made during architecture design

Knowing when verification is complete

Join us for lunch as a panel of industry experts discuss what's really happening inside the companies who are working to shape the multi-die system era.

Panelists

- **Alex Starr,** AMD
- **Arturo Salz,** Synopsys
- **Bharat Vinta,** NVIDIA
- **Divyang Agrawal,** Tenstorrent

Moderated by

- **Lauro Rizzati**

13:30 – 15:00

Workshop: Expanding role of Static Signoff in Verification Coverage
Room: Cascade
Presented by Real Intent

Introduction: Simulation-based testing has been the go-to approach for checking nearly everything through targeted tests in the ever-evolving verification methodologies. Its effectiveness has been undeniable and continues to play a critical role in verification landscape. However, it has its limitations. The number of possibilities it can cover remains limited compared to the complete set of potential behaviors, regardless of the number of tests or clever techniques used.

Today, static verification has become an indispensable companion to simulation, formal methods, and other verification techniques, excelling in various specific applications. Its scope has expanded beyond traditional timing analysis, linting, and clock domain crossing (CDC) checks. This expansion has been made possible by the continuous advancements in the power and versatility of static tools and the growing complexity of modern designs. Some verification challenges that were previously addressed by throwing more resources, such as people, licenses, and machines at the problem, have now surpassed the capabilities of conventional methods for confident signoff.

Summary of the content of the workshop: This workshop explores several emerging static signoff technologies and their applications in verification flows across both large and small design and verification organizations. These technologies are shaping how various companies approach verification coverage, offering valuable insights and efficiencies that complement existing methodologies.

By leveraging the strengths of static verification alongside other verification techniques, engineers and organizations can enhance their verification coverage, ensuring robust and reliable designs in the face of increasing design complexity. As the field continues to evolve, staying up-to-date with the latest static signoff advancements will be crucial in maintaining a competitive edge in the semiconductor industry.

13:30 – 15:00
Workshop: Expanding role of Static Signoff in Verification Coverage (cont.)

The workshop teaches new verification areas where static sign-off methodologies are evolving and getting deployed to increase efficiency and coverage of verification.

- Asynchronous Logic sign-off flows beyond CDC
- DFT Compliance, checking and enabling shift left using static sign-off
- Archiectural Compliance using static sign-off
- Connectivity checking using static-signoff
- Glitch checking metdhology using static-signoff
- Efficient functional sign off by automatic assertion generation for RTL building blocks using static methods
- Advanced methodology to identify X-initialization source errors and fix them to prevent the error from propagating

The workshop then dives deep into specific industry use cases and examples, demonstrating how the industry is adopting these new approaches in the real world.

Nvidia's Asynchronous Logic Sign-Off Flows Beyond Structural CDC Kinara and Alif Semi – Shift Left DFT sign-off methodology for Edge AI Processor Palo Alto Networks - advanced X-propagation methodology to identify X-initialization source errors and fix them to prevent the error from propagating.

Renesas - Efficient functional sign off by automatic assertion generation for RTL building blocks Real Intent with multiple customers – Connectivity, Glitch and architectural compliance using static-signoff. The workshop is designed to benefit audience members and enable them to enhance the state of verification practice in their workplace.

13:30 – 15:00
Workshop: RISC-V Core Verification: A New Normal in Verification Techniques

Room: Donner

Presented by Breker

Speaker: **Adnan Hamid,** CTO, Breker Verification Systems; **John Sotiropoulos,** Principal Engineer, Breker Verification Systems

Abstract: RISC-V processor cores, particularly complex application devices, require verification content that explores scenarios not encountered with other blocks, however complex. However, a lot can be learned by examining these content requirements for many verification situations. This workshop will explore a number of techniques employed on RISC-V cores today and consider how they may be applied across a range of designs.

For complex, multi-core, out-of-order devices, instruction compliance and micro-architecture validation is not enough. Platform-level testing such as asynchronous interrupts, complex load-store and other scenarios are required. Coherency is a factor requiring specialized testing, as well as atomic operation, paging, privilege level switching, PMP security validation, the examples go on and on.

The verification content for RISC-V processor multi-cores may be considered in layers. A classic RISC-V (and indeed other processor core) verification environment might start with some base tests, instruction compliance, and micro-architectural validation before employing a broad range of system integration and infrastructure content that ensures the device can efficiently drive an SoC. Performance issues must be evaluated alongside functional areas, data coherency, load store hazards, interrupt mechanisms are just a few of the examples of areas to be tested. Of course, if security, or low power are requirements, this adds more to the verification load.

13:30 – 15:00

Workshop: RISC-V Core Verification: A New Normal in Verification Techniques (cont.)

This workshop will guide attendees through verification content designed to address these and other scenarios critical for core level verification. A range of test techniques designed to fully cover these scenarios in a concurrent fashion to wring out unpredictable corner cases will be detailed, that are used on real designs today. Using the Accellera Portable Stimulus Standard, the construction of reusable, configurable SystemVIP will be examined to show how tests might be set up for a variety of scenarios across multiple projects.

Not working on a RISC-V core? This workshop will expose verification mechanisms that can be applied to a broad range of blocks for many applications. By experiencing the techniques applied to processor verification a lot can be learned for verification in general.

13:30 – 15:00

Workshop: Automating the Integration Workflow with IP Centric Design

PERFORCE

Room: Siskiyou

Presented by Perforce

Speaker: **Simon Butler,** Helix IPLM, General Manger

Session Abstract: During a project, subsystem and full-chip integration plays a crucial role. Integration can be particularly challenging on large SoCs with distributed teams due to complexity of the integration process, multi-site infrastructure issues, as well as the need to collaborate across multiple time zones. Often, integrators must integrate design blocks delivered by distant teams on which they do not possess any expertise. This causes long lead times with the integration process, repeated debugging of similar issues, and a perpetual state of missing key integration milestones. With IP-centric design and the use of "IP aliases," we propose a methodology that provides a streamlined, controlled, quality-based, and transparent flow that helps teams reliably meet integration milestones and more easily debug integration issues.

Simon Butler is the founder of Methodics Inc., acquired by Perforce in 2020. He is currently the General Manager of the Helix IPLM (formerly Methodics IPLM) business unit at Perforce. Methodics created IP lifecycle management as a new business segment in the enterprise semiconductor space to serve the needs of IP and component-based design. Simon has 30 years of IC design and EDA tool development and specializes in product strategy and design.

2025

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