2026

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DVCON

CONFERENCE AND EXHIBITION

UNITED STATES

# DVCON 2026 UNITED STATES CONFERENCE PROGRAM

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## DVCon U.S. 2026

### Welcome Message from DVCon U.S. General Chair, Xiaolin Chen

**General Chair – Xiaolin Chen, Synopsys**

WIt is my great honor and pleasure to serve as the DVCon U.S. Conference General Chair. On behalf of the steering committee, a warm welcome to DVCon U.S. 2026! This year will be the first time we are at the new venue, the Hyatt Regency, Santa Clara, California, located in the heart of Silicon Valley. I am incredibly pleased to say that this has allowed us to expand the capacity for all the technical session rooms, as well as provide attendees with a much larger exhibition hall.

We are immensely proud to continue our tradition of providing an annual technical forum that serves the practicing design verification community. Now in its 38th year, DVCon U.S. has long established itself as the must-attend premier Design and Verification Conference and Exhibition.

We have an exciting program in store for attendees this year with a fully packed schedule over four days. It should not come as a surprise to anyone that many of the topics will be centered around AI!

We have two extremely exciting Industry keynotes on the schedule. The first keynote on Tuesday afternoon "Verification, Validation and HW/SW Challenges with Complex Chiplet-based Systems" will feature Abhi Kolpekwar, Senior Vice President Digital Verification Technology from Siemens EDA, Jean-Marie Brunet, Senior Vice President Hardware Assisted Verification from Siemens EDA, and a special guest speaker Alon Shtepel, Senior Director ASIC Verification and Emulation from Micron Technology. The second keynote is the Invited Industry Keynote on Wednesday afternoon "From Pixels to Tokens: Chip Design and Verification in the Era of AI" that will be presented by Stuart Oberman, Vice President from Nvidia. Both keynote presentations will offer insights into the vision and direction of design and verification for the future, especially with the disruption to workflows at all levels by AI.

Our panel chair, Ambar Sarkar, has organized a thought-provoking panel session, "Is AI the Key to Ending the Verification Bottleneck?" This will be an opportunity for attendees to participate and interact with panelists by asking questions during a live discussion.

Monday and Thursday will continue to be designated to tutorials and workshops, and I am pleased to share that this year's program features more tutorials and workshops than in previous years. Shekar Chetput, the Tutorial and Workshop Chair has arranged an excellent program for us. The Accellera tutorials and workshops offer the latest in standards development in Clock Domain Crossing, Portable Stimulus, IP-XACT, and SystemVerilog Mixed-signal interfaces, and applications. In addition, many of the other tutorials and workshops are on the topic of agentic AI across RTL design, verification, and debug. I hope you take advantage of these opportunities to take a deeper look at what the industry has to offer and how these products and technologies can be used in methodologies shaping the next generation of electronic system design.

We appreciate all of the submissions to the conference, as we had a record number of submissions this year. Please keep contributing so the whole community can benefit from everyone sharing and learning. Dave Rich, the Technical Program Chair, along with a group of volunteer technical program committee members, have extensively reviewed and selected the best submissions, putting together outstanding technical sessions for attendees. Since AI is pervasive in all the design and verification flows, we have made some changes to the technical session format this year. Instead of having a separate AI track, we have interweaved AI related talks into the respective technologies that can be applied in design and verification projects.

To continue with our new tradition at DVCon U.S., there will be a Poster Ninja Warrior session on Wednesday, which will include the highest rated four posters (voted on by attendees) battling it out for top honors. Each Poster Warrior will be given five minutes to present their poster, followed by an insightful Q&A from a panel of expert judges. Audience participation

and reaction are highly encouraged as it is an integral part of the judging process, creating a dynamic and interactive event.

We look forward to your votes for the best paper and best poster awards at the reception after the last program session on Wednesday.

We hope all the attendees will fully enjoy the keynotes, outstanding technical sessions, networking experience, and the opportunity to preview the latest industry design and verification tools in a variety of exhibitions.

To put together a conference of this magnitude requires tremendous effort. I would like to express my sincere gratitude to the Steering Committee and the Technical Program Committee, with the support of Conference Catalysts, for their tireless efforts to put together an excellent program for attendees. I would also like to thank all the sponsoring organizations for their generous financial support. Lastly, I want to thank all conference participants for their contributions in helping to build the foundation of this conference.

I look forward to seeing you at DVCon U.S. 2026!

**Xiaolin Chen**

**DVCon U.S. 2026 General Chair**

## CONFERENCE SPONSOR

Accellera Systems Initiative is an independent, not-for profit organization dedicated to create, support, promote, and advance system-level design, modelling, and verification standards for use by the worldwide electronics industry. We are composed of a broad range of members that fully support the work of our technical committee to develop technology standards that are balanced, open, and benefit the worldwide electronics industry. Leading companies and semiconductor manufacturers around the world are using our electronic design automation (EDA) and intellectual property (IP) standards in a wide range of projects in numerous application areas to develop consumer, mobile, wireless, automotive, and other "smart" electronic devices. Through an ongoing partnership with the IEEE, standards and technical implementations developed by Accellera Systems Initiative are contributed to the IEEE for formal standardization and ongoing governance.

### Our Mission

At Accellera our mission is to provide a platform in which the electronics industry can collaborate to innovate and deliver global standards that improve design and verification productivity for electronics products.

### The purposes of the organization include:

- Provide design and verification standards required by systems, semiconductor, IP, and design tool companies to enhance a front-end design automation process.
- Collaborate with our community of companies, individuals, and organizations to deliver standards that lower the cost of designing commercial IC and EDA products and embedded system solutions, as well as increase the productivity of designers worldwide.
- Encourage availability and adoption of next-generation EDA and IP standards that encompass system-level, RT-level, and gate-level design flows.
- Collaborate with the electronic design community to deliver standards that increase designer productivity and lower the cost of product development.
- Provide mechanisms that enable the continued growth of the Accellera Systems Initiative user community including SystemC, Universal Verification Methodology (UVM), and IP-XACT.
- Standardize technical implementations developed by Accellera Systems Initiative through the IEEE.

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## DVCon U.S. 2026 - Program Grid

### Monday, March 2, 2026 - Registration opens at 8:30 AM.

| TIME (PST) | Magnolia | Grand Ballroom C | Grand Ballroom D | Grand Ballroom EFGH |
|---|---|---|---|---|
| 9:00-10:30 | **System Validation - It's the Protocol Stupid (Part 1)** SYNOPSYS® | **Liberating Functional Verification from Boolean Shackles** REAL INTENT | **Portable Stimulus Modeling Patterns (Practical Tips for Adopting PSS)** accellera SYSTEMS INITIATIVE | **Venue Set Up** |
| 10:30-11:00 | **Coffee Break** (Grand Ballroom ABCD Foyer) | | | |
| 11:00-12:30 | **System Validation - It's the Protocol Stupid (Part 2)** SYNOPSYS® | **Property Generator: simple generation of Formal Assertion IP** LUBIS EDA | **SystemC – What's New? What's Next?** accellera SYSTEMS INITIATIVE | |
| 12:30-13:30 | **Sponsored Lunch** **From Failing Test to Fix: Agentic Root Cause Analysis for Modern Verification** (Grand Ballroom AB) ChipAgents AI | | | **Exhibitor Set Up** |
| 13:30-15:00 | **AI Agents for Design and Verification: Opportunities and Challenges** ChipAgents AI | **AI Meets Formal: Practical Applications from Industry Leaders** SYNOPSYS® | **TvastaaVP: An agentic AI approach to SystemC (Part 1)** Vayavya Labs Pvt. Ltd. | |
| 15:00-15:30 | **Coffee Break** (Grand Ballroom ABCD Foyer) | | | |
| 15:30-17:00 | **ChipAgents in Practice: Lessons from One Year of Agentic AI EDA Deployment** ChipAgents AI | **Automate the Pain Away: HW/SW Interface Design Methodology** ARTERIS IP | **TvastaaVP: An agentic AI approach to SystemC (Part 2)** Vayavya Labs Pvt. Ltd. | |
| 17:00-18:00 | **Welcome Reception Sponsored by Accellera Systems Initiative** (Grand Ballroom EFGH/Exhibit Hall) accellera SYSTEMS INITIATIVE | | | |

## DVCon U.S. 2026 - Program Grid

### Tuesday, March 3, 2026 - Registration opens at 8:00 AM.

| TIME (PST) | Magnolia | Grand Ballroom C | Grand Ballroom D | Grand Ballroom EFGH |
|---|---|---|---|---|
| 8:30-9:00 | **Opening Session** (Grand Ballroom C) | | | |
| 9:00-10:30 | **1 Accelerating Coverage** | **2 Functional Safety** | **3 Coverage in Memory Design** | |
| 10:30-11:00 | **Coffee Break** (Grand Ballroom ABCD Foyer) | | | |
| 10:30-12:00 | **Poster Session** (Grand Ballroom ABCD Foyer) | | | |
| 12:00-13:00 | **Sponsored Lunch** **From Engines to Intelligence: Managing Verification at Massive Scale** SIEMENS (Grand Ballroom AB) | | | **Exhibit Hall Open** |
| 13:00-14:00 | **Industry Keynote** **Beyond Bigger Designs: Rethinking Verification for the Era of Convergence** SIEMENS (Grand Ballroom CD) | | | |
| 14:00-14:30 | **Coffee Break** (Grand Ballroom EFGH/Exhibit Hall) | | | |
| 14:30-16:30 | **4 Formal Automation** | **5 Security in Design & Verification** | **6 Digital Twin / Emulation Acceleration** | |
| 16:30-18:00 | **Reception** (Grand Ballroom EFGH/Exhibit Hall) | | | |

## DVCon U.S. 2026 - Program Grid

### Wednesday, March 4, 2026 - Registration opens at 8:00 AM.

| TIME (PST) | Magnolia | Grand Ballroom C | Grand Ballroom D | Grand Ballroom EFGH |
|---|---|---|---|---|
| 8:30-9:30 | **Panel** (Grand Ballroom CD) | | | |
| 9:30-10:00 | **Coffee Break** (Grand Ballroom ABCD Foyer) | | | |
| 10:00-12:00 | **7 Formal Verification Innovations** | **8 Automating Verification Insight** | **9 UVM Practices** | |
| 12:00-13:00 | **Sponsored Lunch** **Bridging Minds and Machines: How AI is Transforming the Future of Design Verification** cadence® (Grand Ballroom AB) | | | **Exhibit Hall Open** |
| 13:00-14:00 | **Invite Keynote** **From Pixels to Tokens: Chip Design and Verification in the Era of AI** (Grand Ballroom CD) | | | |
| 14:00-15:00 | **Poster Ninja Session** (Grand Ballroom CD) | | | |
| 15:00-15:30 | **Coffee Break** (Grand Ballroom EFGH/Exhibit Hall) | | | |
| 15:30-17:00 | **10 Regression Management** | **11 Tightening Verification Closure** | **12 Python Integration** | |
| 17:00-18:30 | **Reception & Best Paper Presentation** (Grand Ballroom EFGH/Exhibit Hall) | | | |

## DVCon U.S. 2026 - Program Grid

### Thursday, March 5, 2026 - Registration opens at 8:30 AM.

| TIME (PST) | Ballroom E | Grand Ballroom C | Grand Ballroom D |
|---|---|---|---|
| 9:00-10:30 | Broadening the Adoption of Hardware-Assisted Verification with Next Generation Emulation Appliance<br>cadence® | Agentic AI for RTL Signoff<br>SIEMENS | Breakthrough in CDC-RDC Verification Defining a Standard for Interoperable Abstract Model (Part 1)<br>accellera SYSTEMS INITIATIVE |
| 10:30-11:00 | Coffee Break<br>(Grand Ballroom ABCD Foyer) | | |
| 11:00-12:30 | Verification in the Agentic AI era - a whole new ball game!<br>cadence® | Power Dynamics: Shaping the Future of the Data Centric Era and the Role of AI<br>SIEMENS | Breakthrough in CDC-RDC Verification Defining a Standard for Interoperable Abstract Model (Part 2)<br>accellera SYSTEMS INITIATIVE |
| 12:30-13:30 | Sponsored Lunch<br>Generative AI – Is it Real or Merely a Hallucination?<br>SYNOPSYS®<br>(Grand Ballroom AB) | | |
| 13:30-15:00 | High-Level Synthesis Meets FPGA Prototyping in the Cloud<br>SIEMENS | Transforming Verification Debug: AI Innovations with Verdi<br>SYNOPSYS® | IP-XACT Demystified: An In-Depth Training on the IEEE 1685-2022 IP-XACT Standard<br>accellera SYSTEMS INITIATIVE |

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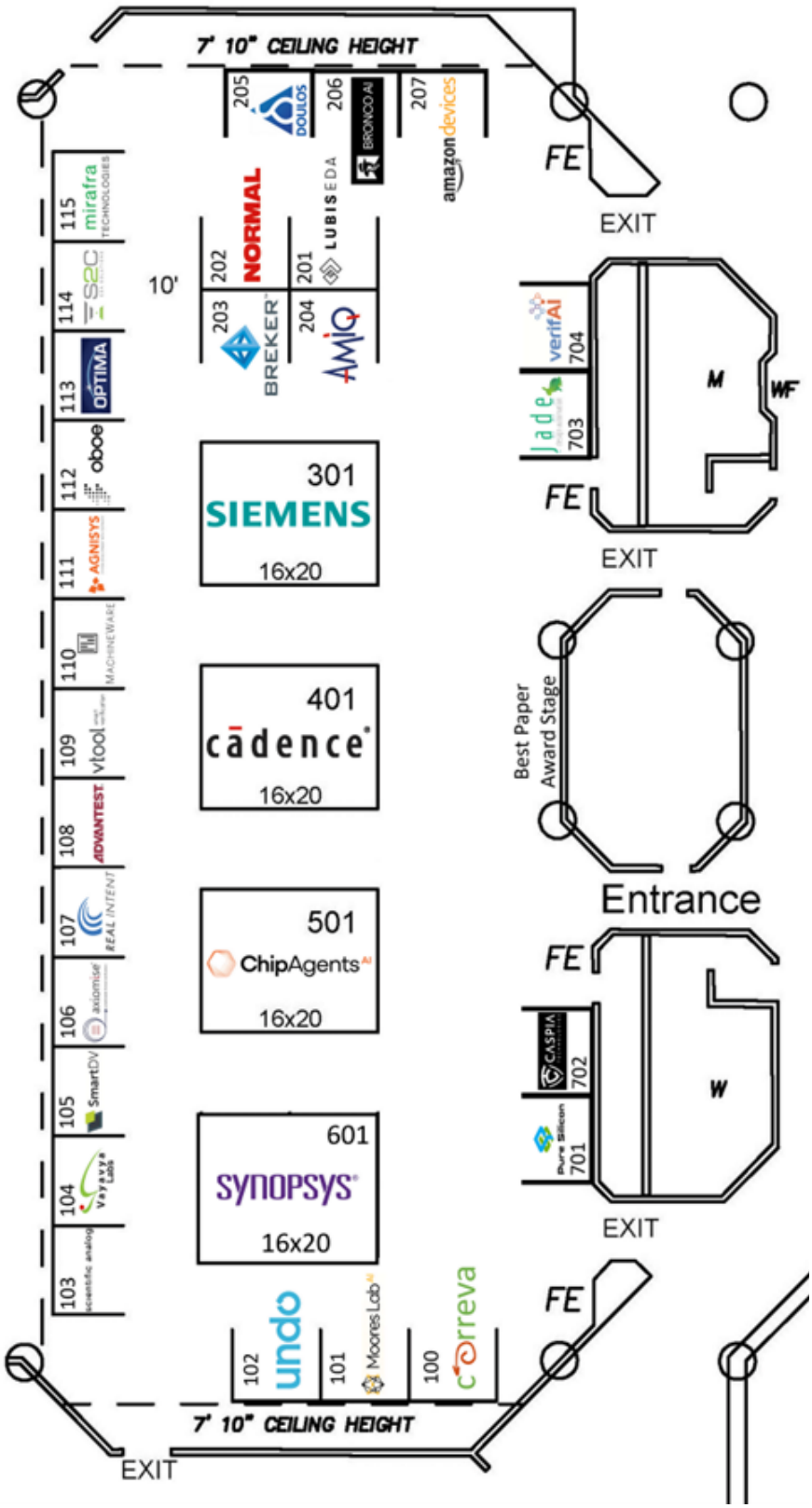
## DVCON U.S. 2026 EXHIBIT HALL MAP



# Technical Program: Monday, March 2
**Time Zone is PST**

## 9:00 – 10:30

### System Validation - It's the Protocol Stupid (Part 1)
**Room: Magnolia**

**Johannes Stahl,** Synopsys; **Rob Parris,** Synopsys

Today's conventional wisdom is that you need the fastest and highest capacity verification engines to tackle the hardware and software complexity of complex multi-die systems. Those teams that are just thinking about these aspects are in for a rough awakening. Without a full range of protocol solutions matching the IP to their verification engines, they can spend months before they can run the 1st system validation test. Participants of this tutorial will learn what it takes to validate a protocol with state-of-the-art solutions.

We will take you through the 10 interface solutions you need to successfully implement and verify interfaces. Each step will include a demo video of the solution. The tutorial will also relate to our demonstration of Hardware-assisted verification on the show floor. Tutorial participants can ask  deep dive questions on the show floor.

## 9:00 – 10:30

### Liberating Functional Verification from Boolean Shackles
**Room: Grand Ballroom C**

**Vikas Sachdeva,** Bangalore

This workshop, titled "Liberating Functional Verification from Boolean Shackles", emphasizes the growing importance of static signoff in early-stage functional verification. It highlights how static methods, unlike traditional Boolean-based simulation and formal techniques, offer faster, scalable, and easier verification—crucial for handling today's complex SoC designs. Covering real-world case studies and best practices, the session demonstrates how early RTL static signoff improves design quality, reduces re-spins, shortens time-to-market, and enhances security. It's aimed at RTL designers, verification engineers, and chip architects seeking efficient, shift-left verification strategies.

## 9:00 – 10:30

### Portable Stimulus Modeling Patterns (Practical Tips for Adopting PSS)
**Room: Grand Ballroom D**

The Portable Stimulus Standard (PSS) offers a scalable solution to the demands of SoC-level verification by enabling engineers to model verification intent at a higher level of abstraction and apply constrained-random techniques at the scenario level. This allows for automated generation of diverse test cases across multiple execution platforms, dramatically improving reuse and coverage.

This workshop will equip attendees with a deeper understanding of PSS fundamentals and demonstrate how to apply it to real-world verification challenges. Through practical examples, participants will learn how PSS can revitalize legacy flows, streamline test creation, and unlock new capabilities for system-level verification. We will cover the following topics:

- Modeling system resource allocation and constraints
- Modeling and automating device configuration
- Reuse and composition of virtual sequences
- Modeling complex coverage
- Realizing PSS scenarios in UVM and C

Whether you're looking to extend your current methodology or future-proof your verification strategy, this session will show how PSS can help you meet today's challenges—and tomorrow's—with confidence.

## 10:30 – 11:00
**Coffee Break**
**Room: Grand Ballroom ABCD Foyer**

## 11:00 – 12:30
**System Validation - It's the Protocol Stupid (Part 2)**
**Room: Magnolia**

**Johannes Stahl,** Synopsys; **Rob Parris,** Synopsys

Today's conventional wisdom is that you need the fastest and highest capacity verification engines to tackle the hardware and software complexity of complex multi-die systems. Those teams that are just thinking about these aspects are in for a rough awakening. Without a full range of protocol solutions matching the IP to their verification engines, they can spend months before they can run the 1st system validation test. Participants of this tutorial will learn what it takes to validate a protocol with state-of-the-art solutions.

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## 11:00 – 12:30
**Property Generator: simple generation of Formal Assertion IP**
**Room: Grand Ballroom C**

**Dr. Tobias Ludwig,** LUBIS EDA

Writing SystemVerilog Assertions (SVA) is a must-do task when applying Formal Verification. Not only is this a highly specialized and manual task, but also fulfilling the completeness-criteria and making sure that the full functionality and state-space of the design is covered can be tricky.

We will introduce the Property Generator, a tool that generates a complete set of SystemVerilog Assertions (SVA) from SystemC-based models. This enables formal verification to begin as early as the virtual prototyping phase. It results in correct-by-construction assertions, quick turn- around in case requirement changes, and, lastly, removes the need for human review of the assertions.

We aim to introduce the tool to a wider audience and help people starting their formal verification journey.

By leveraging state-of-the-art compilers, the Property Generator eliminates the need for manual property creation, accelerating verification workflows and reducing review overhead. This workshop demonstrates how behavioral intent, captured in SystemC, can be directly translated into actionable formal properties, leading to bug-free RTL designs with less manual effort and greater confidence.

## 11:00 – 12:30
**SystemC – What's New? What's Next?**
**Room: Grand Ballroom D**

SystemC has long served as a foundational technology for full-system simulation and virtual platform development. While the standard has matured over many years, the continued evolution of modern system architectures and tooling has made it clear that SystemC must keep advancing to remain effective and interoperable across diverse use cases.

## 11:00 – 12:30

### SystemC – What's New? What's Next? (cont.)

With the release of IEEE 1666 2023, the SystemC base standard has undergone its most significant update in over a decade, strengthening the core features required to build robust, high performance simulators.

However, experience has shown that the base standard alone is not sufficient, especially in scenarios involving complex virtual platforms, where greater unification and standardized mechanisms for tool interaction are increasingly essential.

To address these needs, the SystemC Configuration, Control, and Inspection (CCI) standard has been revitalized. Beyond the configuration capabilities introduced earlier, ongoing work within the CCI Working Group is defining new APIs that provide a standardized approach for inspection and simulator control. These extensions aim to harmonize how tools across vendors access and manipulate SystemC based simulations, reducing fragmentation and enabling more predictable and portable flows.

This presentation will cover:

- The current state of the SystemC standard, with a focus on the updates introduced in IEEE 1666 2023
- An introduction to SystemC CCI, including the goals of the working group and the upcoming standardized APIs for inspection and control
- Lessons learned from widely used open source full system simulation frameworks such as QEMU
- An outlook on the future direction of SystemC and CCI, the challenges facing the industry, and the steps required to overcome them

The session will conclude by leading into a Birds of a Feather (BoF) discussion, inviting participants to help shape the next steps for SystemC and its ecosystem to ensure the community is prepared for the future.

## 12:30 – 13:30

### Lunch Sponsored by ChipAgents AI

**Room: Grand Ballroom AB**

### From Failing Test to Fix: Agentic Root Cause Analysis for Modern Verification

**Zackary Glazewski,** Founding Engineer, ChipAgents.ai; **Mehir Arora,** Head of Engineering, ChipAgents.ai

Root cause analysis (RCA) is one of the most time-consuming and least scalable parts of the verification lifecycle. As SoCs grow exponentially in complexity and regressions span millions of cycles, engineers are left manually correlating waveforms, logs, assertions, and coverage data to answer a deceptively simple question: why did this test fail?

In this session, we introduce an AI-agent–based approach to root cause analysis, developed and deployed in ChipAgents™ and already used in production verification flows at leading semiconductor companies. We will walk through how autonomous AI agents ingest simulation outputs (logs, waveforms, assertions, coverage), reason across design intent and testbench structure, and iteratively narrow failures to actionable root causes, often in minutes instead of days.

Using real-world DV scenarios, we will demonstrate how AI-driven RCA:

- Automatically localizes failure sources across RTL, testbench, and constraints
- Distinguishes symptom signals from true root causes
- Generates explainable hypotheses engineers can validate and fix
- Scales across large regressions without adding human bottlenecks

Attendees will leave with a clear understanding of how AI agents can be integrated into existing verification environments to dramatically reduce debug time, improve first-pass success, and free verification teams to focus on higher-value work.

## 12:30 – 16:30
**Exhibitor Set-Up**
**Room: Grand Ballroom EFGH (Exhibit Hall)**

## 13:30 – 15:00
**AI Agents for Design and Verification: Opportunities and Challenges**
**Room: Magnolia**

**William Wang,** ChipAgents; **Mehir Arora,** ChipAgents; **Kexun Zhang,** ChipAgents

The semiconductor industry faces relentless pressure to shorten design cycles, improve quality, and manage escalating complexity. Traditional EDA tools have made remarkable progress, yet verification still consumes the majority of project schedules and resources. Recent breakthroughs in large language models and agentic AI present a transformative opportunity: autonomous, task-oriented agents that can collaborate with engineers in design and verification workflows.

This workshop explores the promise and limitations of AI agents applied to RTL design, debug, and verification. We will demonstrate how agentic systems can generate UVM testbenches, accelerate coverage closure, and automate tedious debugging tasks, all while integrating seamlessly with existing toolchains through standard EDA workflows. At the same time, we will examine the critical challenges that remain: ensuring correctness and determinism, handling corner cases, and scaling performance across large design teams.

Participants will gain a grounded understanding of where AI agents add real value today, what open problems the community must address, and how engineers can adopt these tools responsibly. Through case studies and interactive discussion, we will highlight early successes, industry feedback, and research directions that could reshape how verification is performed in the next decade.

Whether you are a verification engineer, design engineer, or decision-maker, this session will help you separate hype from reality and envision a future where AI agents become trusted fellow engineers in the chip design process.

## 13:30 – 15:00
**AI Meets Formal: Practical Applications from Industry Leaders**
**Room: Grand Ballroom C**

**Xiaolin Chen,** Synopsys; **Bindumadhava S.S.,** Google; **Ghaith Bany Hamad**, Nvidia; **Pradip Prajapati,** Synopsys

Formal verification offers unmatched rigor in ensuring design correctness, but its adoption is often hindered by steep learning curves, manual effort, and delayed integration into the design flow. This workshop explores how artificial intelligence (AI) is transforming formal verification into a more accessible, scalable, and efficient methodology from the earliest stages of development as well as being weaved through different phases of formal verification. AI can intelligently guide assertion generation, property selection, and proof strategies—dramatically reducing setup time and increasing coverage. By learning from design patterns, verification history, and specification intent, AI enables earlier deployment of formal methods, improves usability for non-experts, and accelerates convergence for seasoned practitioners.

You will hear talks from industry leaders such as Nvidia, Google as well as Synopsys IP showing real-world example usages and results. Attendees will gain practical insights into AI-augmented formal verification workflows that deliver faster results, higher confidence, and reduced human effort. Whether you're a verification engineer, formal expert, or RTL designer, this session will show how to harness AI to make formal easier to adopt and more impactful than ever before.

## 13:30 – 15:00
### TvastaaVP: An agentic AI approach to SystemC (Part 1)
**Room: Grand Ballroom D**


**Shravan Kumar Belagal Math**, Vayavya Labs Pvt Ltd; **Rajat Shetty,** Vayavya Labs Pvt Ltd; **Karthick Gururaj,** Vayavya Labs Pvt Ltd; **Sandeep Pendharkar,** Vayavya Labs Pvt Ltd


The growing complexity of modern semiconductor systems demands rapid and accurate creation of high-fidelity virtual prototypes, such as SystemC-based models, to accelerate early software development and architectural exploration. Traditional model development workflows are highly manual, requiring iterative design documentation, implementation, and validation — often extending over several weeks. To address this, Vayavya introduces TvastaaVP, an Agentic AI methodology that leverages specialized AI agents to automate and orchestrate the SystemC model development lifecycle, thereby significantly reducing turnaround time.

The tutorial demonstrates the methodology to generate SystemC based models from IP/SoC datasheets using Agentic AI workflow. The workshop will show a live demo of LLM based agents in operation, generating complete SystemC model of a peripheral device HMAC – from PDF specification to model code and test implementation.

## 15:00 – 15:30
### Coffee Break
**Room: Grand Ballroom ABCD Foyer**

## 15:30 – 17:00
### ChipAgents in Practice: Lessons from One Year of Agentic AI EDA Deployment
**Room: Magnolia**


**Torin Schlunk,** ChipAgents; **Mehir Arora,** ChipAgents; **William Wang,** ChipAgents; **Luke Frey,** ChipAgents


In the past year, AI agents have moved from research prototypes into production EDA environments. At the forefront of this transition is ChipAgents, an agentic AI system purpose-built for RTL design and verification. Since its introduction, ChipAgents has been deployed across leading semiconductor companies, engaging with design engineers, verification teams, and toolchain owners on real projects. This workshop shares what we have learned from those deployments: the successes, surprises, and lessons that can guide the broader adoption of agentic AI in EDA.

We will present case studies where ChipAgents accelerated UVM testbench development, improved coverage closure, and reduced debug turnaround time, while also discussing scenarios where agents encountered limitations and required human guidance. Particular emphasis will be placed on integration patterns: how ChipAgents accelerate a variety of workflows, how teams structured evaluations, and which workflows benefited most from agentic AI.

Just as importantly, we will cover the challenges discovered in practice: from handling complex corner cases, to measuring ROI, to work with production environments. Audience members will gain an honest perspective on both the potential and the practical hurdles of introducing agentic AI into high-stakes semiconductor design and verification flows.

By distilling insights from one year of real-world usage, this session aims to equip engineers, managers, and researchers with actionable knowledge on how to evaluate, adopt, and scale AI agents responsibly in their own verification environments.

# Technical Program: Monday, March 2 (cont.)
**Time Zone is PST**

## 15:30 – 17:00

**Automate the Pain Away: HW/SW Interface Design Methodology**
**Room: Grand Ballroom C**

**Tim Schneider,** Arteris; I**nsaf Meliane,** Arteris; **Alvin Santos,** Arteris

Modern System on Chip (SoC) designs involve many components: Hardware Description Languages (VHDL, System Verilog), Unified Power Format (UPF), Software Languages (C#/C++), Interconnect standards (IPXACT, AMBA) and purpose built layers such as the Universal Verification Methodology (UVM) and System Verilog Assertions (SVA).

This tutorial explores SoC Integration technologies to ""blend"" these components together, proposing a more efficient methodology to increase productivity and ensure first-time SoC project success. The example design combines RISC-V processor elements, Arteris IP and AMBA Peripherals, "blending" together the various standards such as CSRSpec, System Verilog, UPF and IP-XACT into a complete SoC system. Index Terms – SoC Integration; IP-XACT; System Verilog; UVM; Hardware Software Interface, RISC-V.

## 15:30 – 17:00

**TvastaaVP: An agentic AI approach to SystemC (Part 2)**
**Room: Grand Ballroom D**

**Shravan Kumar Belagal Math,** Vayavya Labs Pvt Ltd; **Rajat Shetty,** Vayavya Labs Pvt Ltd; **Karthick Gururaj,** Vayavya Labs Pvt Ltd; **Sandeep Pendharkar,** Vayavya Labs Pvt Ltd

The growing complexity of modern semiconductor systems demands rapid and accurate creation of high-fidelity virtual prototypes, such as SystemC-based models, to accelerate early software development and architectural exploration. Traditional model development workflows are highly manual, requiring iterative design documentation, implementation, and validation — often extending over several weeks. To address this, Vayavya introduces TvastaaVP, an Agentic AI methodology that leverages specialized AI agents to automate and orchestrate the SystemC model development lifecycle, thereby significantly reducing turnaround time.

The tutorial demonstrates the methodology to generate SystemC based models from IP/SoC datasheets using Agentic AI workflow. The workshop will show a live demo of LLM based agents in operation, generating complete SystemC model of a peripheral device HMAC – from PDF specification to model code and test implementation.

## 17:00 – 18:00

**Welcome Reception Sponsored by Accellera Systems Initiative**
**Room: Grand Ballroom EFGH (Exhibit Hall)**

## Technical Program: Tuesday, March 3
**Time Zone is PST**

### 8:30 – 9:00
**Opening Session**
**Room: Grand Ballroom C**

### 9:00 – 10:30
**1 Accelerating Coverage**
**Room: Magnolia**

Session Chair: **Jamie Ridgeway**

[102] AI Driven Advanced Debugging in SoC Design Verification

**Shreya Jayatheerth Joshi,** Samsung Semiconductors India R&D; **Alok Kumar,** Samsung Semiconductors India R&D; **Poonam Shettar,** Samsung Semiconductors India R&D; **Sanjoy Saha,** Samsung Semiconductors India R&D; **Shrinidhi S Rao,** Samsung Semiconductors India R&D; **Garima Srivastava,** Samsung Semiconductors India R&D

[123] Streamlining RAL-based Cross-Coverage and Sequence Coverage through Automation

**Vijayakrishnan Rousseau,** Intel Corporation; **Satyajit Sinari,** Intel Corporation; **Ram Immaneni,** Intel Corporation; **Mangayarkarasi Arumugam,** Intel Corporation; **Raghavendra CK,** Intel Corporation; **Prasad Shah,** Intel Corporation

[111] Beyond Heuristics: AI/ML Driven Verification for Design Sign-off

**Gulshan Sharma,** Samsung Semiconductor India Research; **Sougata Bhattacharjee,** Samsung Semiconductor India Research; **Avinash Bollu,** Samsung Semiconductor India Research; **Abhishek Raj,** Samsung Semiconductor India Research; **Akshaya Jain,** Samsung Semiconductor India Research

### 9:00 – 10:30
**2 Functional Safety**
**Room: Grand Ballroom C**

Session Chair: **Tom Fitzpatrick**

[176] Early FMEDA at RTL for Functional Safety, Correlating RTL Metrics to GLS for Accurate Architectural Analysis

**MyungKyoon Yim**, Hyundai; **Vedant Garg,** Synopsys; **Buyong Um,** Hyundai; **Kyle Kim,** Synopsys; **Liz Song,** Synopsys

[174] Closing the Safety Verification Loop, FMEDA-Driven Fault Simulation and Advanced Debug for Efficient Fault Classification

**Sagar Hema Vidya,** AMD; Vedant Garg, Synopsys; **Sudhakar Chappidi,** AMD; **Sharon monica Kurmana,** AMD

[94] Optimizing Functional Fault Grading Flow for Memory Designs

**Euisang Yoon,** Siemens EDA; **Arun Gogineni,** SiemensEDA; **Eunjong Oh,** Samsung Electronics; **Seongwook Lee,** Samsung Electronics; **Sungyun Yoo,** Siemens EDA; **Geonbeom Kwon,** Siemens EDA; **Yoseop Lee,** Samsung Electronics; **Hyojin Choi,** Samsung Electronics; **Saurabh Srivastava,** Siemens EDA

## Technical Program: Tuesday, March 3 (cont.)
**Time Zone is PST**

### 9:00 – 10:30
**3 Coverage in Memory Design**
**Room: Grand Ballroom D**

Session Chair: **Karan Arora**

[84] A GPT-2 Tabular Transformer Model for Automated DRAM Verification

**Lorenzo Ferretti,** Micron Technology; **Chinmaya Behera,** Micron Technology; **Shailesh Sharma,** Micron Technology; **Nihar Athreyas,** Micron Technology; **Vikram Narayan,** Micron Technology; **Samir Mittal,** Micron Technology

[89] From Specification to Closure: A Semi-Automated Coverage-Driven Verification Methodology for Cache Coherent Home Nodes

**Kavin Rajendran,** OPENEDGES Square, Corp.; **Anish mon Soosai,** OPENEDGES Square, Corp.; **Kranthi Konganti,** OPENEDGES Square, Corp.; **Shivaprasad Naranapura Chandrashekara Swamy,** OPENEDGES Square, Corp.

[63] A Platform-Based Approach to Reduce Verification Turn-Around Time in Memory Designs

**Junho An,** Samsung Electronics; **Seonyong Lee,** Samsung Electronics; **Gyehyun Na,** Samsung Electronics; **Minseon Kim,** Samsung Electronics; **Dongeun Lee,** Samsung Electronics; **Jaehyun Park,** Synopsys; **Kiuk Kim,** Synopsys

### 10:30 – 11:00
**Coffee Break**
**Room: Grand Ballroom ABCD Foyer**

### 10:30 – 12:00
**Poster Session**
**Room: Grand Ballroom ABCD Foyer**

[23] Application of Metamorphic Testing to Mixed Signal Systems with Behavioral Models

**Daniel Cross,** Cadence Design Systems

[28] Taming Configuration Complexity: A UVM-Based Approach To IP Verification

**Bhaskar Vedula,** Intel Corporation; **Ganesh Sharma,** Intel Corporation; **Stephen Haake,** Intel Corporation; **Chandrakanth Betageri,** Intel Corporation

[38] Elementary Subpart Extraction, Enabling True Shift-left in Safety Analysis for Closing Architectural Vulnerabilities and Reducing Fault Injection Iterations

**Luc Baudoin,** AMD; **Vedant Garg,** Synopsys

[51] Accelerating SDC Coverage Closure Using ML and LLM-Based Approaches

**Seungkyu Baek,** Samsung Foundry; **Jiyong Kwon,** Samsung Foundry; **Jaein Hong,** Samsung Foundry; **Sungcheol Park,** Samsung Foundry

[53] Multi-Agent Orchestration for Autonomous Regression Management

**Sangwoo Noh,** Samsung; **Jin Choi,** Samsung; Seunghee Yim, Samsung

[62] There and Back Again: Simulation-to-Synthesis Scenario Reuse with PSS

**Tom Fitzpatrick,** Big Fish EDA

[64] Towards Self-Adaptive SoC Design Verification: KG-Enhanced Generative AI, RL and Backpropagation Debugging

**Insu Jang,** Samsung Electronics; **Seonghee Yim,** Samsung Electronics; **Hanna Jang,** Samsung Electronics; **Seonil Brian Choi,** Samsung Electronics

## 10:30 – 12:00
**Poster Session (cont.)**

[68] An Efficient Random Instruction Sequence Generation for Verification of Domain Specific Architecture Processor

**Wonjae Lee,** Samsung Electronics Co., Ltd.; **Youngsub Ko,** Samsung Electronics Co., Ltd.; **Yelim Han,** Samsung Electronics Co., Ltd.; **Doowon Lee,** Samsung Electronics Co., Ltd.; **Dahyun Yoo,** Samsung Electronics Co., Ltd.; **Heewon Ahn,** Samsung Electronics Co., Ltd.; **Joongbaik Kim,** Samsung Electronics Co., Ltd.

[71] Integrating Formal Methods with Lightweight Testing for Automotive Firmware Verification

**Bryan Olmos,** Infineon Technologies Dresden AG & Co. KG; **Shuhang Zhang,** Infineon Technologies AG; **Wolfgang Kunz,** Rheinland-Pfälzische Technische Universität Kaiserslautern-Landau; **Djones Lettnin,** Infineon Technologies AG

[81] RTL Performance Isn't Just a Number - It's a Story

**Olivera Stojanovic,** Vtool; **Hagai Arbel,** Vtool

[85] plusargs++: Make Plusargs Great … Like They Never Were Before

**Bryan Morris,** Ciena Corp; **Michael Silveira,** Ciena Corp

[92] An Approach to Create Scalable Power Management Verification Environment

**Pranav Mopkar,** Intel Corporation

[98] AI Agent-based Specification Matching System for SoC RTL Verification

**Yonghyun Kwon,** Samsung Electronics; **Hanna Jang,** Samsung Electronics; **Seonghee Yim,** Samsung Electronics

[122] RISC-V reuse made easy by interface generation and integration automation

**Ares Tahiraga,** Infineon Technologies; **Said Llukaj,** Infineon Technologies; **Wei Zhao,** Infineon Technologies; **Endri Kaja,** Infineon Technologies; **Sebastian Prebeck,** Infineon Technologies; **Wolfgang Ecker,** Infineon Technologies

[134] Saarthi for AGI: Towards Domain-Specific General Intelligence for Formal Verification

**Aman Kumar,** Infineon Technologies India Private Limited; **Deepak Narayan Gadde,** Infineon Technologies Dresden AG & Co. KG; **Minh Luu,** Infineon Technologies Vietnam Company Ltd.; **Keerthan Kopparam Radhakrishna,** Infineon Technologies Dresden AG & Co. KG; **Vaisakh Naduvodi Viswambharan,** Infineon Technologies Dresden AG & Co. KG; **Sivaram Pothireddypalli,** Infineon Technologies India Private Limited

[147] GLS Shift Over Through Timing Constraint Verification: A Comprehensive Framework

**Amey Telang,** Samsung Semicondutor India Research; **Sunil Kashide,** Samsung Semicondutor India Research; **Garima Srivastava,** Samsung Semicondutor India Research; **Shekhar Sharma,** Samsung Semicondutor India Research; **Karishma Singh,** Cadence

[165] IP-XACT Based PSS Modeling for Shift-Left SoC Verification

**Moonki Jang,** Samsung Electronics Co.,Ltd; **Yonghyun Yang,** Samsung Electronics Co.,Ltd; **Kangho Lee,** Samsung Electronics Co.,Ltd; **Yejin Lee,** Samsung Electronics Co.,Ltd; **Youngchan Lee,** Samsung Electronics Co.,Ltd; **Sunil Roe,** Samsung Electronics Co.,Ltd; **Youngsik Kim,** Samsung Electronics Co.,Ltd; Seonil Choi

## 12:00 – 18:00
**Exhibit Hall Open**
**Room: Grand Ballroom EFGH (Exhibit Hall)**

## 12:00 – 13:00

SIEMENS

**Lunch Sponsored by Siemens**
**Room: Grand Ballroom AB**

**From Engines to Intelligence: Managing Verification at Massive Scale**

**Harry Foster, Darron May, Vijay Chobisa**

As chip designs grow more complex and software-driven, verification teams are running more engines, larger regressions, and deeper analyses than ever before—yet achieving confidence and closure often feels harder, not easier.

In this Siemens EDA–sponsored luncheon panel, industry experts and practitioners discuss how verification is evolving as designs scale beyond the practical limits of any single engine. Panelists will share the challenges of coordinating simulation, formal, emulation, prototyping, and verification data, along with the pragmatic approaches teams use today—combining advanced commercial solutions with in-house workflows layered on existing platforms.

Looking ahead, the discussion explores the shift from raw engine output to intelligence, including the role of AI technologies and emerging agentic approaches. The panel will examine how these capabilities are being explored—and in some cases applied—to interpret results, prioritize risk, and help verification engineers sustain confidence as scale continues to increase.

## 13:00 – 14:00

SIEMENS

**Industry Keynote: Beyond Bigger Designs: Rethinking Verification for the Era of Convergence**
**Room: Grand Ballroom CD**

**Abhi Kolpekwar,** Sr. Vice President, Digital Verification Technology, Siemens EDA;
**Jean-Marie Brunet,** Sr. Vice President, Hardware Assisted Verification, Siemens EDA;
**Alon Shtepel,** Senior Director, ASIC Verification and Emulation, Micron Technology

As semiconductor systems evolve toward software-defined, AI-driven, and increasingly modular architectures, verification challenges are no longer driven solely by design size. Instead, correctness increasingly emerges from interacting behaviors—across hardware and software, power and performance states, workloads, and execution platforms—transforming verification from a linear, phase-based activity into a continuous, feedback-driven process.

This keynote brings together three complementary perspectives to examine this shift. An architectural view explores how the meaning of complexity has changed, as interacting system behaviors and iterative verification loops increasingly shape productivity limits beyond what isolated optimizations can address. A hardware-assisted verification perspective examines why faithful execution across simulation and acceleration platforms is essential to expose these behaviors. A practitioner's perspective then grounds these ideas in real-world experience, describing how a large engineering organization is integrating generative and agentic AI into its verification flows, the challenges of doing so consistently at scale, and the open questions that remain—how to measure productivity, ensure quality, and build trust.

Together, these perspectives highlight why future verification approaches must be connected across silos, data-driven across iterations, and scalable in human judgment to reason holistically about system behavior throughout the product lifecycle.

# Technical Program: Tuesday, March 3 (cont.)
**Time Zone is PST**

## 14:00 – 14:30
**Coffee Break**
**Room: Grand Ballroom EFGH (Exhibit Hall)**

## 14:30 – 16:30
**4 Formal Automation**
**Room: Magnolia**

Session Chair: **Ankit Garg**

[88] Scalable Formal Verification Framework for NoC System Address Map Configurations

**Anish mon Soosai,** OPENEDGES Square, Corp; **Shivaprasad Naranapura Chandrashekara Swamy,** OPENEDGES Square, Corp; **Kavin Rajendran,** OPENEDGES Square, Corp; **Kranthi Konganti,** OPENEDGES Square, Corp

[194] SIGMA: Sign-off Intelligence with GenAI for Methodical Assurance in Formal Verification

**R C Sanjay Krushnan,** CADENCE DESIGN SYSTEMS INDIA PVT LTD; **Moola Jeevan Chaitanya Goud,** CADENCE DESIGN SYSTEMS INDIA PVT LTD; **Sakthivel Ramaiah,** CADENCE DESIGN SYSTEMS INDIA PVT LTD; **Erik Seligman,** CADENCE DESIGN SYSTEMS

[135] DUET: Agentic Design Understanding via Experimentation and Testing

**Gus Smith,** ChipStack; **Chandra Bhagavatula,** ChipStack; **Vineet Thumuluri,** ChipStack; **Sandesh Adhikary,** ChipStack; **Vivek Pandit,** ChipStack

[14] FVDebug: An LLM-Driven Debugging Assistant for Automated Root Cause Analysis of Formal Verification Failures

**Yunsheng Bai,** NVIDIA; **Ghaith Bany Hamad,** NVIDIA; **Chia-Tung (Mark) Ho,** NVIDIA; **Syed Suhaib,** NVIDIA; **Haoxing (Mark) Ren,** NVIDIA

## 14:30 – 16:30
**5 Secuirty in Design & Verificaiton**
**Room: Grand Ballroom C**

Session Chair: **Peter George**

[182] Effective Methodologies to Accelerate Security Verification

**Lee Anthony Grajo,** Analog Devices; **Ponnambalam Lakshmanan,** Analog Devices; Anders Nordstrom, Cycuity

[143] LFSR: Beyond the Sequential - Unlocking the Potential of Immediate Nth Cycle Output

**Kshiteej Kosambia,** Cadence; **Prakash Darji,** Cadence

[47] Security Verification in Practice: Lessons from Pre-Silicon Analysis of SoC Subsystems

**Yashwanth Kumar,** Marvell Technology, Inc.; **Rachana Maitra,** Marvell Technology, Inc.

[121] Threat Modeling for SoC Security Design: IEEE P3164 SA-EDI Standardization

**Wenzhen Li,** IEEE P3164

## 14:30 – 16:30

**6 Digital Twin / Emulation Acceleration**
Room: Grand Ballroom D

Session Chair: **Harry Foster**

[57] Enhancing Automotive ECU Design with Digital Twin Simulation: Comparative Study of Virtual Platform, FPGA Prototyping, and Edge Device Configurations

**Sara Abd AlWahab,** Electronics and Communications Engineering Department, Cairo University; **Mohamed AbdElsalam,** Siemens Digital Industries Software; **Ahmed H. Khalil,** Electronics and Communications Engineering Department, Cairo University; **Hassan Mostafa,** Electronics and Communications Engineering Department, Cairo University

[69] An AI Agent Framework with Elasticsearch for Scalable Post-Silicon Debug Automation

**Minuk Lee,** Samsung Electronics; **Hanna Jang,** Samsung Electronics; **Seonghee Yim,** Samsung Electronics; **Youngsik Kim,** Samsung Electronics

[79] AI-Driven Adaptive Emulation for Accelerated Pre-Silicon Debug: High-Fidelity Silicon Replay

**Sampathkumar M Ballary,** Samsung Semiconductor India Research; **Priyadarshini Pai,** Samsung Semiconductor India Research; **Aruna S Lohiya,** Samsung Semiconductor India Research; **Ramesh G Patgar,** Samsung Semiconductor India Research; **Karthik Srinivasan,** Samsung Semiconductor India Research; **Vemuri Krishna Sumanth,** Samsung Semiconductor India Research; **Vandana S,** Samsung Semiconductor India Research; **Venkata Subba Rao Manne,** Samsung Semiconductor India Research; **Subrata Sarkar,** Samsung Semiconductor India Research; **Samruddhi C R**

[166] Accelerating Bare Metal Driver Development with Linux Drivers and System Verilog DPI-C.

**Suchir Gupta,** Synopsys; Amit Sharma, Synopsys; **Suneetha Suryadevara,** Synopsys; **Vishnuvardhan Reddy,** Synopsys

## 16:30 – 18:00

**Reception**
**Room: Grand Ballroom EFGH (Exhibit Hall)**

# Full Program – Wednesday, March 4
**Time Zone is PST**

## 8:30 – 9:30
### Panel: Is AI the Key to Ending the Verification Bottleneck?"
**Room: Grand Ballroom CD**

Moderator: **Vishal Karna,** Senior Director of Engineering, Qualcomm Technologies

Panelist: **Igor Markov,** Professor and AI/EDA Researcher, Synopsys; **Dr. Shahid Ikram,** Formal Verification Architect, Altera Corp.; **Tao Liu,** Verification Lead, OpenAI; **Hamid Shojaei,** Distinguished Engineer, Cadence Design Systems

Verification is the largest driver of time and cost in modern semiconductor projects, often consuming up to two-thirds of total development effort. Debugging and coverage closure dominate this workload, creating long, iterative loops between design and verification teams. Traditionally, "shift left" methodologies have sought to empower designers to verify more of their own work earlier in the cycle—but steep learning curves for verification tools have limited adoption.

AI—especially large language model (LLM)-powered assistants—offers a new way forward. These tools can generate complete, high-quality verification assets from natural-language design intent, automate simulation and formal runs, and produce actionable debug reports in minutes. Advocates see this as the breakthrough that will make "design with verification" a reality. Skeptics question whether AI can handle the complexity, corner cases, and predictability demands of industrial-scale verification.

This panel will bring together leaders in AI, EDA, and semiconductor design to debate whether AI is truly the key to ending the verification bottleneck—or just the next over-hyped technology.

## 9:30 – 10:00
### Coffee Break
**Room: Grand Ballroom ABCD Foyer**

## 10:00 – 12:00
### 7 Formal Verification Innovations
**Room: Magnolia**

Session Chair: **Vibarajan Viswanathan**

[127] A New Methodology for Formal Equivalence Checking of Sorting Algorithms

**Emiliano Morini,** NVIDIA

[25] ConnChecker: Automated Root-Cause Analysis for Formal Connectivity Check via Graph

**Ngoc Tiep Do,** Infineon Technologies; **Linh Anh Nguyen,** Cornell University; **Danh Minh Luu,** Infineon Technologies

[65] Early Deep Bug Discovery via Re-run Acceleration and Parallel Multi-Depth BMC Exploration

**Jungwoo Seo,** Samsung Electronics Co., Ltd.; **Dongyoung Kim,** Samsung Electronics Co., Ltd.; **Sungjin Park,** Siemens EDA; **Mark Eslinger,** Siemens EDA; **Juyeon Son,** Samsung Electronics Co., Ltd.; **Gyehyun Na,** Samsung Electronics Co., Ltd.; **Dongeun Lee,** Samsung Electronics Co., Ltd.

[58] Scaling Formal Verification of Network On Chip Using Path Decomposition

**Bilal Ahmed,** 10x Engineers; **Umar Yaqoob,** 10x Engineers; **Bilal Zafar,** 10x Engineers; **Misbahud Din,** Lahore University of Management and Sciences

# Full Program – Wednesday, March 4 (cont.)
**Time Zone is PST**

## 10:00 – 12:00
### 8 Automating Verification Insight
**Room: Grand Ballroom C**

Session Chair: **Santosh Kumar**

[118] EVM - Enhanced Verbosity Methodology

**Gergő Vékony,** ARM; **József Mózer,** ARM

[124] Automated Root-Cause Analysis of GPU Pipeline Corruptions in Graphics and Compute Workloads

**Pravesh Dangwal,** Intel; **Himanshu Somaiya,** Intel; **Leena Singh,** Intel

[181] A Novel ML-driven simulation Log Debugger

**Narasimha Rao Chinni,** Samsung semiconductor india research; **Sunil Shriragrao Kashide,** Samsung semiconductor india research; **Garima Srivastava,** Samsung semiconductor india research

[139] Passive Token Accounting: Managing LLM Cost in Continuous Verification

**Ajith Jose,** Dhenara Inc

## 10:00 – 12:00
### 9 UVM Practices
**Room: Grand Ballroom D**

Session Chair: **Paul Marriott**

[164] Visualizing SystemVerilog and UVM

**Jamie Ridgeway,** Paradigm Works

[34] Integrating RTL design and UVM Testbench with Hyperledger Blockchain and Machine Learning for better efficiency and optimization

**Sougata Bhattacharjee,** Samsung Semiconductor India Research

[91] Exploring UVM TLM2 based Sequence, Sequencer and Driver in UVM

**Neha Goyal,** Nvidia Corporation; Justin Refice, Nvidia Corp

[26] Harnessing Volatility: Innovative Strategies for Register Synchronization in UVM RAL

**Bhaskar Vedula,** Intel Corporation; **Stephen Haake P,** Intel Corporation; **Chandrakanth Betageri,** Intel Corporation

## 12:00 – 13:00
### Lunch Sponsored by Cadence
**Room: Grand Ballroom AB**

cadence®

Bridging Minds and Machines: How AI is Transforming the Future of Design Verification

Moderator: **Jin Zhang,** Cadence

Panelist: **Sai Mai,** OpenAI

Panelist: **Amita Trisal,** Qualcomm

Let's discuss over lunch how artificial intelligence is transforming hardware verification. We'll explore the evolution of AI and machine learning tools that are making verification smarter, more efficient, and more accessible—paving the way toward zero-bug silicon. Our aim is to understand how these advancements are shaping the future and what they mean for verification engineers today and in the future.

## Full Program – Wednesday, March 4 (cont.)
**Time Zone is PST**

### 12:00 – 18:30
**Exhibit Hall Open**
**Room: Grand Ballroom EFGH (Exhibit Hall)**

### 13:00 – 14:00
**Invited Keynote: From Pixels to Tokens: Chip Design and Verification in the Era of AI**
Room: Grand Ballroom CD

**Stuart Oberman,** Vice President, GPU Hardware Engineering, Nvidia

GPUs have evolved from large 3D graphics accelerators into massively parallel programmable processors optimized for accelerating GenAI training and inference. With Moore's law ended, generational gains now rely on aggressive architectural innovation within strict power, thermal, and cost constraints, even as design size, software content, and heterogeneity continue to grow. At the same time, first-silicon success is approaching statistical impossibility as traditional verification flows struggle with software-driven behavior and an exploding state space. Drawing on two decades of experience building GPUs along this trajectory, this talk will examine how design and verification tools and methodologies have adapted to manage both exploding complexity and a sharply increasing development cadence, and how emerging AI-driven agentic workflows across RTL design and verification are becoming essential to sustain the push toward ever more complex GPUs and SoCs on ever faster schedules.

### 14:00 – 15:00
**Poster Ninja Session**
**Room: Grand Ballroom CD**

### 15:00 – 15:30
**Coffee Break**
**Room: Grand Ballroom EFGH (Exhibit Hall)**

### 15:30 – 17:00
**10 Regression Management**
**Room: Magnolia**

Session Chair: **Kamel Belhous**

[54] A 3-Tiered Agentic AI Framework for Verification Regression

**Jin Choi,** Samsung Electronics; **Sangwoo Noh,** Samsung Electronics; **Seunghee Yim,** Samsung Electronics

[52] A Novel Fast Regression: An AI/ML Driven Automated Sanity Regression Flow

**Joonho Chung,** Samsung Electronics; **Daeseo Cha,** Samsung Electronics; **Woojoo Space Kim,** Samsung Electronics; **Youngsik Kim,** Samsung Electronics; **Seonil Brian Choi,** Samsung Electronics; **Nili Segal,** Cadence Design Systems

[117] Etabot: Multi Agent Verification Management with Chat Accessible Midpoint Metrics and Finish-Date Forecasts

**Zili Fang,** Silicon Labs

## Full Program – Wednesday, March 4 (cont.)
**Time Zone is PST**

### 15:30 – 17:00
**11 Tightening Verification Closure**
**Room: Grand Ballroom C**

Session Chair: **Benjamin Ting**

[177] Real-Time Performance Insights: AI-Accelerated Trace-Driven Analysis for Multi-GPU Pre-Silicon Verification Environments
**Vinoth Selvan,** NVIDIA Corporation; **Prashanth Rajan,** NVIDIA Corporation

[19] Database Driven RTL Simulation: Fighting Billion-Gate Verification Bottlenecks
**Victor Besyakov,** BTA Design Services

[67] Unified AI-Driven Verification: Combining Spec-RAG, Memory Networks, and Generative AI
**Seonghee Yim,** Samsung Electronics; **Insu Jang,** Samsung Electronics; **Hanna Jang,** Samsung Electronics; **Seonil Brian Choi,** Samsung Electronics

### 15:30 – 17:00
**12 Python Integration**
**Room: Grand Ballroom D**

Session Chair: **Bhaskar Vedula**

[149] Properly Introducing Python to your UVM Testbench
**Matthew Ballance,** AMD

[46] Breaking the Wait: Customizable, Real-Time Post-Processing for Data Integrity Verification in SerDes Systems
**Chandana K Nallangi,** Intel; **Suresh S Gandhi,** Intel

[22] A Modern Debug Paradigm: Python Visualization For DDR Memory Controller's Performance Analysis
**Pallavi Kumar,** AMD; Michael Chan, AMD

### 17:00 – 18:30
**Reception & Best Paper Presentation**
**Room: Grand Ballroom EFGH (Exhibit Hall)**

## Full Program – Thursday, March 5th
**Time Zone is PST**

### 9:00 – 10:30
**Broadening the Adoption of Hardware-Assisted Verification with Next Generation Emulation Appliance**
**Room: Ballroom E**

**Rohan Ganpati,** Cadence Design Systems; **Michael Young,** Cadence Design Systems; **Lance Tamura,** Cadence Design Systems; **William Wei,** Skymizer

The rapid growth in semiconductor design activity is projected to increase in the coming years, however, RTL design and verification remains a significant challenge in semiconductor development. While emulation is widely adopted to accelerate verification, today, most emulation technologies cater to the needs of large-scale 'billion-gate' class designs.

Many design teams across various organizations create IP or small-scale yet mission-critical ASIC/SoC designs and strive to leverage emulation. Unfortunately, existing emulation solutions are often inaccessible to these teams due to constraints such as limited capital budgets, low priority in resource allocation, or lack of data center infrastructure.

To lower the barrier of adoption, Cadence introduced the Dynamic Duo System Studio, comprising the Palladium Z3 System Studio and the Protium X3 System Studio. The Palladium Z3 System Studio is a standalone emulation appliance tailored to emulate designs up to 128 million gates, with software and tool flows compatible with the enterprise-scale Palladium Z3 system.

In this session, we intend to present the benefits and features of the Palladium Z3 System Studio-- a leading-edge emulation appliance that significantly lowers the adoption barrier for design and verification teams, enabling them to accelerate hardware/software co-verification workloads via emulation.

We also intend to share case studies from companies specializing in AI chip development and other mission-critical applications. These case studies will demonstrate how design teams achieved multi-thousand-fold performance improvements over simulation, shortened verification cycles, and accelerated software bring-up by several months through the adoption of System Studio into their workflows.

### 9:00 – 10:30
**Agentic AI for RTL Signoff**
**Room: Grand Ballroom C**

**Darron May,** Siemens EDA; **Ronen Shoham,** Siemens EDA; **Joe Hupcey III,** Siemens EDA

The escalating complexity of modern System-on-Chip (SoC) designs challenges traditional RTL signoff, creating bottlenecks in design creation and RTL signoff. This tutorial introduces a transformative paradigm: applying Agentic AI to intelligently automate and optimize the entire design-to-signoff process, moving beyond static flows to a dynamic, intelligent ecosystem that's capable of autonomous reasoning and adaptation; supporting engineers from initial concept and design exploration through final, comprehensive verification.

Central to this strategy is the novel Model Context Protocol (MCP), a standardized semantic communication layer that transforms IC design and verification tools into active, context-aware participants by exposing real-time design state, creation parameters, and tool capabilities. This enables a rich, shared understanding, allowing tools to publish critical information and respond intelligently, effectively merging design exploration and verification.

## 9:00 – 10:30

### Agentic AI for RTL Signoff (cont.)

Leveraging MCP, platform-agnostic Agentic AI frameworks orchestrate complex tasks across design and verification domains. These agents are empowered to reason, plan, adapt, and execute strategies dynamically. They assist in design space exploration, architectural optimization, rapid iteration, identifying critical verification paths, generating targeted stimulus, intelligent debug, and root-cause analysis with minimal human intervention. This drives significant acceleration for design and verification closure, reducing cycle times and improving signoff quality.

The approach is engineer-centric, providing intuitive guidance to configure and deploy these advanced AI capabilities, fostering a collaborative human-AI partnership. This tutorial will detail the architectural principles behind this Agentic AI approach, demonstrating how MCP facilitates interoperability and enables autonomous, trusted RTL signoff. Attendees will gain insights into fostering design quality and liberating engineers from repetitive tasks.

## 9:00 – 10:30

### Breakthrough in CDC-RDC Verification Defining a Standard for Interoperable Abstract Model (Part 1)

**Room: Grand Ballroom D**

accellera SYSTEMS INITIATIVE

**Jean-Christophe Brignone,** STMicroelectronics; **Farhad Ahmed,** Siemens; **Anupam Bakshi,** Agnisys; **Chetan Choppali Sudarshan,** Marvell; **Bill Gascoyne,** Blue Pearl Solutions; **Don Mills,** Arm; **Iredamola Olopade,** Google; **Devendra Gupta,** Agnisys

CDC-RDC analysis has evolved as an inevitable stage in RTL quality signoff in the last two decades. Over this period, the designs have grown exponentially to SOC's having 2 trillion+ transistors and chiplet's having 7+ SOC's.

Different vendor tool abstracts are seen because of multiple IP vendors, even in house teams might deliver abstracts generated with different vendors tools.

The Accellera CDC Working-Group aims to define a standard CDC-RDC IP-XACT / TCL model to be portable and reusable regardless of the involved verification tool.

As moving from monolithic designs to IP/SOC with IPs sourced from a small/select providers to sourcing IPs globally (to create differentiated products), the quality must be maintained as driving faster time-to-market. In areas where the standards (SystemVerilog, OVM/UVM, LP/UPF) are present, the integration is able to meet the above (quality, speed). However, in areas where standards (in this case, CDC-RDC) are not available, most options trade-off either quality, or time-to-market, or both :-( Creating a standard for inter-operable collateral addresses this gap.

This tutorial aims to remind the definitions of CDC-RDC Basic Concepts and constraints, as well as the description of the reference verification flow, and addressing the goals, scope, structure & deliverables of the Accellera CDC Working Group in order to elaborate a specification of the standard abstract model.

A status related to the last LRM version open to public review by 2025-Q4, will be presented.

## 10:30 – 11:00

### Coffee Break

**Room: Grand Ballroom ABCD Foyer**

## 11:00 – 12:30

### Verification in the Agentic AI era - a whole new ball game!

**Room: Ballroom E**

cadence®

**Moshik Rubin,** Cadence Design Systems; **Yael Abarbanel,** Cadence Design Systems

Autonomous AI agents are ushering in a new era for verification by offloading work traditionally performed by CAD teams and expert DV/FV engineers. These autonomous agents use specifications, design related data, and verification context—combined with seamless access to Cadence tools and internal data models—to autonomously generate verification collaterals and execute verification tasks with unprecedented efficiency, consistency, and quality.

This session will introduce the Cadence Agentic Verification, a coordinated multi-agent system orchestrated with Cadence's verification platforms to achieve full-scale DV and FV goals. These autonomous agents generate comprehensive verification environments—or upgrade existing ones—incorporating all required verification collateral, such as UVM testbenches, SystemVerilog assertions, and verification plans, with full traceability back to the product specification. Central to this approach is a mental model derived from the product specification and RTL, that captures design intent, functional behavior, interface protocols, and boundary conditions, providing a rich contextual foundation that guides agent reasoning. Engineers can refine this model using natural language, while it simultaneously accelerates agent autonomy and deepens the verification team's understanding of the design.

We will also showcase advancements in Cadence Verisium AI that extend autonomy into regression and debug, including intelligent testcase selection, regression orchestration, AI driven failure triage, bug pattern prediction, and context-aware waveform root cause analysis.

By combining autonomous agents with the Cadence data models, engines, and domain expertise, our solutions dramatically improve engineering efficiency, accelerate verification signoff, and enhance silicon quality—sparing verification teams the time to focus on architecture and innovation

## 11:00 – 12:30

### Power Dynamics: Shaping the future of the data centric era and the role of AI

**Room: Grand Ballroom C**

SIEMENS

**Amir Attarha,** Siemens

From battery operated handhelds to datacenter servers, electronic devices are defined by their power characteristics. Depending on the application area, total power consumption varies based on the semiconductor (SoC) content used, and the intended purpose for the device. One truth applies to every SoC, power analysis requires a holistic methodology from architectural exploration to tape-out to accurately addresses power concerns.

One of the key factors used to calculate power consumption is the dynamic power that has become increasingly important in technologies such as FinFET. Here the gate area has increased; hence, the load capacitance is larger and the impact of the switching power more pronounced.

In this workshop, join us in exploring the power dynamics shaping the future of the data centric era, with a focus on the growing influence of artificial intelligence. We'll examine emerging methodologies for power profiling and analysis and their positive impact on meeting power requirements and how AI is transforming the way we approach SoC power.

## 11:00 – 12:30

### Breakthrough in CDC-RDC Verification Defining a Standard for Interoperable Abstract Model (Part 2)

**Room: Grand Ballroom D**

**Jean-Christophe Brignone,** STMicroelectronics; **Farhad Ahmed,** Siemens; **Anupam Bakshi,** Agnisys; **Chetan Choppali Sudarshan,** Marvell; **Bill Gascoyne,** Blue Pearl Solutions; **Don Mills,** Arm; **Iredamola Olopade,** Google; **Devendra Gupta,** Agnisys

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## 12:30 – 13:30

### Lunch Sponsored by Synopsys

**Room: Grand Ballroom AB**

**Generative AI: Is it Real or Merely a Hallucination?**

Generative AI is reshaping the landscape of design and verification, but separating genuine breakthroughs from hype remains a challenge. As artificial intelligence becomes increasingly embedded in our daily workflows—from voice assistants to autonomous systems—the question arises: is generative AI delivering real, practical value in chip design verification, or are we chasing illusions? And, with the advent of Large Language Models (LLM) and Generative Pre-Trained Transformer (GPT) models, what are the possibilities in design verification?

This session will examine the current state of generative AI in design and verification. We'll explore where Synopsys is investing in agentic solutions and what technology is being implemented in production environments by end users, delivering significant productivity boosts and automation. Join us to discover whether generative AI is truly revolutionizing the industry—or if it's still more hallucination than reality.

## 13:30 – 15:00

### High-Level Synthesis Meets FPGA Prototyping in the Cloud

**Room: Ballroom E**

**Sivasankar Palaniappan,** Siemens EDA; **Mark Azadpour,** AWS

High-Level Synthesis (HLS) is an established design methodology that raises the abstraction level for design and verification. Verification at the abstract level runs much faster than RTL level simulations. But abstract simulations cannot completely verify the implementation, as it omits certain RTL details. For a complete verification, some verification must be performed at the RTL level.

## 13:30 – 15:00
### High-Level Synthesis Meets FPGA Prototyping in the Cloud (cont.)

This talk will describe a design flow that enables FPGA prototype verification of an HLS synthesized module using an Amazon AWS F2 instance as the FPGA prototyping system. AWS F2 instances provide 8 AMD Virtex UltraScale+ HBM VU47P FPGAs on a PCIe card, with DPI and C++ interfaces. The HLS synthesized RTL module is run through the Xilinx tools to program the FPGAs. The HLS C++ testbench, and its associated results checking and coverage, can be reused to with the module loaded into the FPGAs. This enables the proven testbench environment from the HLS flow to be used with a full RTL implementation of the module. Bus interfaces, memories, and interrupt logic can all be modeled and verified at the RTL level, these structures are often abstracted away in High-Level Verification flows. FPGA prototyping can be an ideal complement to High-Level Verification in an HLS design flow. Using cloud-based FPGA instances on AWS eliminates the need for hardware acquisition and management, and can scale up and down as needed based on verification demands.

## 13:30 – 15:00
### Transforming Verification Debug: AI Innovations with Verdi
**Room: Grand Ballroom C**


**Chun Chan,** Synopsys

This session highlights breakthrough AI-powered advancements in debug workflows for RTL design and verification, featuring state-of-the-art capabilities of the Synopsys Verdi platform. Attendees will learn how Verdi's intelligent technology leverages sophisticated artificial intelligence (AI) to enhance collaborative problem-solving, streamline data analysis, and facilitate multi-level debug across simulation, emulation, formal, and static verification environments. Integration with Synopsys verification tools and popular development environments enables users to interact with Verdi for a range of investigative and diagnostic tasks.

Through practical examples and a live demonstration, the session will showcase how next-generation AI can accelerate root cause analysis, suggest effective solutions, and enable comprehensive, data-driven debug strategies. Key features—including advanced interactivity, context-aware analysis, and innovative workflow integration—will be explored. Participants will see how Verdi platform's cutting-edge AI capabilities are transforming the debug process for modern silicon development.

## 13:30 – 15:00
### IP-XACT Demystified: An In-Depth Training on the IEEE 1685-2022 IP-XACT Standard
**Room: Grand Ballroom D**


**Georgios Passas,** Arteris; **Aiyush Aggarwal,** Agnisys; **Freddy Nunez,** Agnisys; **Thomas Burg,** STMicroelectronics; **Richard Weber,** Arteris

As System-on-Chip (SoC) designs grow in scale and complexity, integration teams face significant challenges in managing registers, memory maps, IP packaging, and verification collateral. Traditional methods based on spreadsheets or proprietary formats often result in inconsistencies, delays, and costly rework.

IEEE 1685-2022 (IP-XACT), developed by Accellera, provides a vendor-neutral framework to describe, package, and integrate IP. The 2022 revision introduces an updated schema, richer register and memory map support, and enhanced mechanisms for capturing hierarchy and connectivity. These improvements enable consistent design data exchange across design, verification, and software teams, while supporting greater automation and reuse.

This training workshop provides participants with a practical understanding of IP- XACT 2022 and how to apply it in real SoC projects.

2027

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