PROGRAM AT A GLANCE

Sunday, October 29, 2023

Time	Gallery III
07:30	Registration Open
08:00	CADathlon Breakfast
08:30	
08:30	CADathlon
08:30	
08:30	AM Break
08:30	
08:30	CADathlon
08:30	
08:30	CADathlon
08:30	
08:30	CADathlon
08:30	
08:30	PM Break
08:30	
08:30	CADathlon
08:30	
08:30	
08:30	

PROGRAM AT A GLANCE

2023 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN
IEEE/ACM ICCAD
42nd Edition

See Appendix A & B for Full Session Titles

Monday, October 30, 2023

Time	Sculptor	Artisan	Atelier I	Atelier II	Gallery III
07:00	Speakers Breakfast (Gallery III)				
07:30					
08:00	Opening & Keynote: Bill Dally (Gallery II)				
08:30					
09:00					
09:30	Coffee Break (Gallery III)				
10:00	**Reconf-LP 3** Session Chairs: Vojtech Razek Weikang Qian	**SS 1** Session Chairs: Yibo Lin Cheng Zhuo	**Analog 1** Session Chairs: Zheng Zhang, Liang Chen	**Timing 2** Session Chair: Biying Xu	
10:30					
11:00	**#730, #749, #409, #603**	**#42, #52, #57, ##***	**#413, #886, #455, #393**	**#371, #612, #642, #853**	
11:30	Lunch (Gallery III)				
12:00					
12:30	**Security-Alg 2** Session Chair: Siddarth Garg	**SS 2** Session Chair: Haoyu Yang	**NewComp 1** Session Chair: Saptadeep Pal	**AI-Sys 5** Session Chair: Marina Zapater, Jiaqi Gu	**SRC Poster Session (Gallery III)**
13:00					
13:30	**#717, #363, #942, #924**	**#31, #35, #51, #55**	**#298, #349, #1037, #131**	**#26, #615, #590, #62**	
14:00	**Security Arch 1** Session Chairs: Ramya Jayaram Masti Anupam Chattopadhyay	**SS 3** Session Chairs: Xiaofan Zhang, Peipei Zhou	**Nano 1** Session Chair: Mehdi B. Tahoori	**AI-Tools 2** Session Chairs: Ashutosh Dhar, Chen Zhang	
14:30					
15:00	**#231, #16, #638, #226**	*See Appendix B for session titles*	**#573, #130, #421, #928**	**#214, #229, #367, #411**	
15:30	Coffee Break (Gallery III)				
16:00	**PD 1** Session Chair: Haocheng Li	**SS 4** Session Chairs: Bo Yuan, Jiang Hu	**Bio 1** Session Chair: Mohammed Ibrahim	**SysDesign 1** Session Chair: Hao Zheng	
16:30		#40, #41, ##*, ##*			
17:00	**#114, #137, #510, #601**		**#621, #339, #745, #402**	**#5, #927, #560, #365**	
17:30	**PD 2** Session Chair: Tsung-Yi Ho	**CPS 2** Session Chair: Caiwen Ding	**LLM-Aided Design Panel**	**SysDesign 2** Session Chair: Bei Yu	
18:00					
18:30	**#267, #280, #219, #843**	**#61, #40, #39, #721**		**#680, #87, #266, #281**	
19:00	**Industry Sponsored Session**	**Student Research Competition**			
19:30					
20:00					
20:30	TPC Reception (Gallery III)				
21:00					
21:30					

PROGRAM AT A GLANCE

2023 IEEE/ACM INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN — ICCAD — 42nd Edition

Tuesday, October 31, 2023

Time	Sculptor	Artisan	Atelier I	Atelier II
07:00 – 07:30	**Speakers Breakfast (Gallery III)**			
08:00 – 09:30	**HLS 1** Session Chair: Cunxi Yu **#204, #292, #331, #437, #482**	**SS 5** Session Chair: Xiaoxuan Yang **#30, #34, #36, #44, ##***	**Security-Alg 1** Session Chairs: Satwik Patnaik Amin Rezaei **#974, #286, #727, #713,#319**	**AI-Tools 1** Session Chair: Debjit Sinha **#63, #186, #353, #428, #498**
10:00	**Coffee Break (Gallery III)**			
10:30 – 12:00	**Test 1** Session Chair: Vidya Chhabria **#10, #161, #743, #528, #475**	**Tutorial:** Session Chairs: Xin-Chuan, Kevin Rasch, Shavindra Premaratne **#33: Introduction to Hybrid Quantum-Classical Programming Using C++ Quantum Extension**	**Reconf-LP 1** Session Chairs: Georgios Zervakis, Aoyang Zhang **#1020, #235, #734, #752, #420**	**AI-Sys 1** Session Chairs: Hyoukjou Kwon, Ziyun Li **#511, #258, #96, #422, #256**
12:30 – 13:30	**Keynote Lunch (Gallery II)** ***Ticketed Event - Limited Accessed: First Come, First Served**			
14:00 – 15:00	**Security-Arch 2** Session Chairs: Nimisha Limaye, Jeremy Blackstone **#697, #631, #141, #228**	**NewComp 2** Session Chair: Tsung-Wei Huang **#132, #224, #225, #352**	**Security-Arch 3** Session Chairs: Patanjali SLPSK **#692, #75, #792, #540**	**Analog 2** Session Chair: Sheldon Tan **#494, #307, #683, #154**
15:30	**Coffee Break (Gallery III)**			
16:00 – 17:30	**Timing 1** Session Chairs: Siddhartha Nath, Masanori Hashimoto **#57, #486, #847, #276, #468**	**SS 7: 2023 CAD Contest at ICCAD** Session Chairs: Chun-Yao Wang, Andy Yu-Guang Chen **#48, #39, #32, #53, #56**	**ICCAD Contest for Machine Learning on Hardware (MLHW Contest)**	**AI-Sys 2** Session Chairs: Bingzhe Li, Syed Shakib Sarwar **#120, #451, #343, #746, #308**
18:00 – 21:00	**Job Fair & SIGDA Dinner (Gallery III)**			

PROGRAM AT A GLANCE

2023 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN
IEEE/ACM ICCAD 42nd Edition

Wednesday, November 1, 2023

	Sculptor	Artisan	Atelier I	Atelier II	Curator
07:00 07:30	**Speakers Breakfast (Gallery III)**				
08:00 08:30	**Opening & Keynote: (Gallery II)**				
09:00 09:30 10:00	**NewComp 3** Session Chair: Hussam Amrouch **#178, #446, #449, #487**	**SS 8** Session Chair: Dr. Mark Ren **#43, #46, ##*, ##***	**PD 3** Session Chair: Nima Karimpour Darav **#138, #324, #354, #381**	**SysDesign 3** Session Chair: Xueqing Li **#1018, #912, #1031**	**Top Picks in Hardware & Embedded Security**
10:30	**Coffee Break (Gallery III)**				
11:00 11:30 12:00 12:30	**HLS 2** Session Chair: Ing-Chao Lin **#403, #213, #566, #593, #691**	**Tutorial:** Session Chairs: Chris Lavin, Eddie Hung **#37: RapidWright: Unleashing the Full Power of FPGA Technology with Domain-Specific Tooling**	**AI-Tools 3** Session Chairs: Jihye Kwon, Uday Mallappa **#614, #744, #985, #967, #537**	**AI-Sys 3** Session Chairs: Zhenge Jia, Umamaheswara Rao Tida **#594, #708, #646, #363, #956**	**Top Picks in Hardware & Embedded Security**
13:00 13:30	**Lunch (Gallery III)**				
14:00 14:30 15:00 15:30	**Test 2** Session Chair: Aman Arora **#185, #151, #844, #779, #562**	**SS10** Session Chair: Yiyu Shi **##*, ##*, ##*, #38, #50**	**AI-Tools 4** Session Chairs: Kishor Kunal **#508, #619, #700, #823, #1006**	**AI-Sys 4** Session Chair: Cheng TAN **#955, #1002, #993, #695, #685**	**Top Picks in Hardware & Embedded Security**
16:00	**Coffee Break (Gallery III)**				
16:30 17:00 17:30 18:00	**DFM 1** Session Chair: Takashi Sato **#767, #577, #505, #737, #434**	**SS 11** Session Chairs: Francesco Regazzoni, Apostolos Fournaris **#45, #47, #49, #54, ##***	**Reconf-LP 2** Session Chairs: Eli Bozorgzadeh **#197, #329, #493, #834, #979**	**CPS 1** Session Chair: Meng Li **#1030, #4, #239, #328, #1032**	**Top Picks in Hardware & Embedded Security**

PROGRAM AT A GLANCE: Appendix A

Session Title	Papers
SysDesign 1: **DESIGNING CHIPLET-BASED SYSTEMS**	#5, ARIES: Accelerating Distributed Training in Chiplet-based Systems via Flexible Interconnects #927, Monad: Towards Cost-effective Specialization for Chiplet-based Spatial Accelerators #560, RONet: Scaling GPU System with Silicon Photonic Chiplet #365, Thermally-aware Multi-core Chiplet Stacking
SysDesign 2: **SYSTEM-LEVEL DESIGN AND EXPLORATION**	#680, Path-based Processing using In-Memory Systolic Arrays for Accelerating Data-Intensive Applications #87, PANDA: Architecture-Level Power Evaluation by Unifying Analytical and Machine Learning Solutions #266, A Transfer Learning Framework for High-accurate Cross-workload Design Space Exploration of CPU #281, A General Wavelength-Routed Optical Networks-on-Chip Model with Applications to Provably Good Customized and Fault-Tolerant Topology Designs
SysDesign 3: **DESIGNING MEMORY AND STORAGE SYSTEMS**	#1018, Exploring Error Bits for Memory Failure Prediction: An In-Depth Correlative Study #912, SSDe: FPGA-based SSD Express Emulation Framework #1031, HF-Dedupe: Hierarchical Fingerprint Scheme for High Efficiency Data Deduplication on Flash-based Storage Systems
CPS 1: **Efficient Machine Learning for Real-World Applications**	#1030, TRAIN: A Reinforcement Learning Based Timing-Aware Neural Inference on Intermittent Systems #4, HyperNode: An Efficient Node Classification Framework Using HyperDimensional Computing #239, Brain-inspired Trustworthy Hyperdimensional Computing with Efficient Uncertainty Quantification #328, EDS-SLAM: An Energy-efficient Accelerator for Real-time Dense Stereo SLAM with Learned Feature Matching #1032, MOC: Multi-Objective Mobile CPU-GPU Co-optimization for Power-efficient DNN Inference
CPS 2: **Fast and Trustworthy Embedded Systems**	#61, Data Recomputation for Multithreaded Applications #40, HAPIC: a Scalable, Lightweight and Reactive Cache for Persistent-Memory-based Index #39, DOMINO: Domain-Invariant Hyperdimensional Classification for Multi-Sensor Time Series Data #721, PARseL: Towards a Verified Root-of-Trust over seL4

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AI-Tools 1: **Towards graph-learning assisted electronic design automation (EDA)**	#63: Robust GNN-based Representation Learning for HLS #186: Accelerating Exact Combinatorial Optimization via RL-based Initialization -- A Case Study in Scheduling #353: Memory-aware Scheduling for Complex Wired Networks with Iterative Graph Optimization #428: GraPhSyM: Graph Physical Synthesis Model #498: GRAFT: Graph-assisted Reinforcement learning for Automated SSD Firmware Testing
AI-Tools 2: **Alternative approaches to effective and efficient training of neural networks**	#214: Towards Effective Training of Robust Spiking Recurrent Neural Networks under General Input Noise via Provable Analysis #229: Analog or Digital In-memory Computing? Benchmarking through Quantitative Modeling #367: Falcon: Accelerating Homomorphically Encrypted Convolutions for Efficient Private Mobile Networks Inference #411: Rapid-INR: Storage Efficient CPU-free DNN Training Using Implicit Neural Representation
AI-Tools 3: **Anywhere Anytime – Full Stack AI Deployment**	#614, DeepGate2: Functionality-Aware Circuit Representation Learning #744, DiviML: A Module-based Heuristic for Mapping Neural Networks onto Heterogeneous Platforms #985, PRIMO: A Full-Stack Processing-in-DRAM Emulation Framework for Machine Learning Workloads #967, ARES: A Mapping Framework of DNNs towards Diverse PIMs with General Abstractions #537, Learned Formal Proof Strengthening for Efficient Hardware Verification
AI-Tools 4: **Adaptation, Acceleration, Automation – Tripple-A AI Computing** **16:30**	#508, Automatic Kernel Generation for Large Language Models on Deep Learning Accelerators #619, SATformer: Transformer-Based UNSAT Core Learning #700, GPT4AIGChip: Towards Next-Generation AI Accelerator Design Automation via Large Language Models #823, 3DNN-Xplorer: A Machine Learning Framework for Design Space Exploration of Heterogeneous 3D DNN Accelerators #1006, Klotski: DNN Model Orchestration Framework for Dataflow Architecture Accelerators
AI-Sys 1: **Efficient Accelerator Design**	#511, An Energy-Efficient 3D Point Cloud Neural Network Accelerator With Efficient Filter Pruning, MLP Fusion, and Dual-Stream Sampling #258, BOOST: Block Minifloat-Based On-Device CNN Training Accelerator with Transfer Learning #96, SpOctA: A 3D Sparse Convolution Accelerator with Octree-Encoding-Based Map Search and Inherent Sparsity-Aware Processing #422, RNA-ViT: Reduced-Dimension Approximate Normalized Attention Vision Transformers for Latency Efficient Private Inference #256, SAGA: Sparsity-Agnostic Graph Convolutional Network Acceleration with Near-optimal Workload Balance

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AI-Sys 2: **Design Tools and Performance Optimization for DNN Acceleration**	#120, Improving Realistic Worst-Case Performance of NVCiM DNN Accelerators through Training with Right-Censored Gaussian Noise #451, Runtime Row/Column Activation Pruning for ReRAM-based Processing-in-Memory DNN Accelerators #343, An Open Source Mixed-Precision Neural Network Accelerator Design Framework for FPGAs #746, Accel-GCN: High-Performance GPU Accelerator Design for Graph Convolution Networks #308, MirrorNet: A TEE-Friendly Framework for Secure On-device DNN Inference
AI-Sys 3: **Efficient and Fair Machine Learning on the Edge**	#594, Fluid Batching: Exit-Aware Preemptive Serving of Early-Exit Neural Networks on Edge NPUs #708, Edge-MoE: Memory-Efficient Multi-Task Vision Transformer Architecture with Task-level Sparsity via Mixture-of-Experts #646, FET-OPU: A Flexible and Efficient FPGA-based Overlay Processor for Transformer Networks #636, PP-Transformer: Enable Efficient Deployment of Transformers through Pattern Pruning #956, Fast and Fair Medical AI on the Edge through Neural Architecture Search for Hybrid Vision Models
AI-Sys 4: **Software/Hardware Co-design of AI Accelerator**	#955, SOLE: Hardware-Software Co-design of Softmax and LayerNorm for Efficient Transformer Inference #1002, TSTC: Two-level Sparsity Tensor Core Enabling both Algorithm Flexibility and Hardware Efficiency #993, A Point Transformer Accelerator with Fine-Grained Pipelines and Distribution-Aware Dynamic FPS #695, INR-Arch: A Dataflow Architecture and Compiler for Arbitrary-Order Gradient Computations in Implicit Neural Representation Processing #685, Efficient Sampling and Grouping Acceleration for Point Cloud Deep Learning via Single Coordinate Comparison
AI-Sys 5: **Machine Learning on Emerging Platforms**	#26, Reliable Hyperdimensional Reasoning on Unreliable Emerging Technologies #615, NearUni: Near-Unitary Training for Efficient Optical Neural Networks #590, Kernel Shape Control for Row-Efficient Convolution on Processing-In-Memory Arrays #62, FIONA: Photonic-Electronic Co-Simulation Framework and Transferable Prototyping for Photonic Accelerator

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Reconf-LP 1 **Hot Microarchitectures: Modeling and Design**	#1020, ACOR: On the Design of Energy-Efficient Autocorrelation for Emerging Edge Applications #235, Fast Full-Chip Parametric Thermal Analysis Based on Enhanced Physics Enforced Neural Networks #734, DiCA: A Hardware-Software Co-Design for Differential Check-Pointing in Intermittently Powered Devices #752, IT-DSE: Invariant Risk Minimized Transfer Microarchitecture Design Space Exploration #420, Real-time Thermal Map Estimation for AMD Multi-Core CPUs using Transformer
Reconf-LP 2 **Reconfigurable Computing**	#197, FLEX : Introducing FLEXible Execution on CGRA with Spatio-Temporal Vector Dataflow #329, Meltrix: A RRAM-based Polymorphic Architecture Enhanced by Function Synthesis #493, VecPAC: A Vectorizable and Precision-Aware CGRA #834, AIM: Accelerating Arbitrary-precision Integer Multiplication on Heterogeneous Reconfigurable Computing Platform Versal ACAP #979, IIBLAST: Speeding Up Commercial FPGA Routing by Decoupling and Mitigating the Intra-CLB Bottleneck
Reconf-LP 3 **Approximate Computing**	#730, Bespoke Approximation of Multiplication-Accumulation and Activation Targeting Printed Multilayer Perceptrons #749, DASALS: Differentiable Architecture Search-driven Approximate Logic Synthesis #409, Constant Coefficient Multipliers Using Self-Similarity-Based Hybrid Binary-Unary Computing #603, Xel-FPGAs: An End-to-End Automated Exploration Framework for Approximate Accelerators in FPGA-Based Systems
Security-Alg 1 **IP and IC Trust: Reflections and Advancement**	#974, Reflections on trusting TrustHUB #286, Automated Hardware Trojan Detection at LUT Using Explainable Graph Neural Networks #727, Risk-Aware and Explainable Framework for Ensuring Guaranteed Coverage in Evolving Hardware Trojan Detection #713, PDNSig: Identifying Multi-Tenant Cloud FPGAs with Power Distribution Network-based Signatures #319, An Anti-removal-attack Hardware Watermarking Method based on Polymorphic Gates
Security-Alg 2 **Efficiency for Security**	#717, Striving for Both Quality and Speed: Logic Synthesis for Practical Garbled Circuits #363, EMSim+: Accelerating Electromagnetic Security Evaluation with Generative Adversarial Network #942, Hyperdimensional Computing as a Rescue for Efficient Privacy-Preserving Machine Learning-as-a-Service #924, PSOFuzz: Fuzzing Processors with Particle Swarm Optimization

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Security Arch 1 **Microarchitectural security: to speculate or not?**	#231, BeKnight: Guarding against Information Leakage in Speculatively Updated Branch Predictor #16, HidFix: Efficient Mitigation of Cache-based Spectre Attacks through Hidden Rollbacks #638, Exploration and Exploitation of Hidden PMU Events #226, Secure-by-Construction Design Methodology for CPUs: Implementing Secure Speculation on the RTL'
Security Arch 2 **How do we patch our neural nets (against information leakage)?**	#697, Side Channel-assisted Inference Attack on Machine Learning-based ECG Classification #631, THE-V: Verifiable Privacy-Preserving Neural Network via Trusted Homomorphic Execution #141, Deep-learning Model Extraction through Software-based Power Sidechannel
Security Arch 3 **Microelectronics security: what lies ahead?**	#692, Protection Against Physical Attacks Through Self-Destructive Polymorphic Latch #75, SAM: A Scalable Accelerator for Number Theoretic Transform Using Multi-Dimensional Decomposition #792, KyberMat: Efficient Hardware Accelerator for Matrix-Vector Multiplication in CRYSTALS-Kyber Scheme via NTT and Polyphase Decomposition #540, CRYSTALS-Dilithium on RISC-V Processor: Lightweight Secure Boot using Post Quantum Digital Signature
HLS 1 **Novel ideas in logic synthesis**	#204, Fast Exact NPN Classification with Influence-aided Canonical Form #292, LIM-GEN: A Data-guided Framework for Automated Generation of Heterogeneous Logic-in-Memory Architecture #331, EasySO: Exploration-enhanced Reinforcement Learning for Logic Synthesis Sequence Optimization and a Comprehensive RL Environment #437, MiniTNtk: An Exact Synthesis-based Method for Minimizing Transistor Network #482, WolFEx: Word-Level Function Extraction and Simplification from Gate-Level Arithmetic Circuits
HLS 2 **Technology Mapping revived**	#403, MapBuf: Simultaneous Technology Mapping and Buffer Insertion for HLS Performance Optimization #213, EffiSyn: Efficient Logic Synthesis with Dynamic Scoring and Pruning #566, EasyMap: Improving Technology Mapping via Exploration-Enhanced Heuristics and Adaptive Sequencing #593, AlphaSyn: Logic Synthesis Optimization with Efficient Monte Carlo Tree Search #691, Technology Mapping Using Multi-output Library Cells

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Test 1: **Simulation and Emulation**	#10, Fast and Scalable Gate-level Simulation in Massively Parallel Systems #161, SurgeFuzz: Surge-Aware Directed Fuzzing for CPU Designs #743, TaintFuzzer: SoC Security Verification using Taint Inference-enabled Fuzzing #528, Checkpoint Placement for Systematic Fault-Injection Campaigns #475, Sphinx: A Hybrid Boolean Processor-FPGA Hardware Emulation System
Test 2: **Advances in Verification**	#185, Integrating Exact Simulation into Sweeping for Datapath Combinational Equivalence Checking #151, Verification of Flow-Based Computing Systems using Bounded Model Checking #844, Efficient Formal Verification and Debugging of Arithmetic Divider Circuits #779, Automatic Inductive Invariant Generation for Scalable Dataflow Circuit Verification #562, Accurate Hybrid Delay Models for Dynamic Timing Analysis
PD 1: **Routability and Congestion Prediction**	#114: Routability Prediction and Optimization Using Explainable AI #137: Routablity-driven Orientation-aware Analytical Placement for System in Package #510: Lay-Net: Grafting Netlist Knowledge on Layout-Based Congestion Prediction #601: ClusterNet: Routing Congestion Prediction and Optimization using Netlist Clustering and Graph Neural Networks
PD 2: **Advanced Floorplanning and Partitioning**	#267: Handling Orientation and Aspect Ratio of Modules in Electrostaticsbased Large Scale Fixed-Outline Floorplanning #280: Floorplanning for Embedded Multi-die Interconnect Bridge Packages #219: iPL-3D: A Novel Bilevel Programming Model for Die-to-Die Placement #843: An Open-Source Constraints-Driven General Partitioning Multi-Tool for VLSI Physical Design
PD 3: **The state-of-the-art Placement**	#138: HyPlace-3D: A Hybrid Placement Approach for 3D ICs Using Space Transformation Technique #324: Clock Tree Aware Global Placement for Low Power #354: Stronger Mixed-Size Placement Backbone Considering Second-Order Information #381: Systolic Array Placement on FPGAs

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Timing 1: **Analyzing and Optimizing for PPA, Timing and Reliability**	#57, MasterRTL: A Pre-Synthesis PPA Estimation Framework for Any RTL Design #486, Local Layout Effect-aware Static Timing Analysis by use of a New Sensitivity-based Library #847, Risk Propagation Aware Vector Profiling for High Coverage Dynamic IR-drop Analysis #276, Design and Technology Co-optimization for Useful Skew Scheduling on Multi-bit Flip-flops #468, READ: Reliability-Enhanced Accelerator Dataflow Optimization using Critical Input Pattern Reduction
Timing 2: **Routing and Routability Enhancement**	#371, Towards Timing-Driven Routing: An Efficient Learning Based Geometric Approach #612, NeuroEscape: Ordered Escape Routing via Monte-Carlo Tree Search and Neural Network #642, Delay-Matching Routing for Advanced Packages #853, Power Distribution Network Optimization Using HLA-GCN for Routability Enhancement
DFM 1: **Revolutionalizing Design for Reliability and Manufacturability**	#767, Frequency-Domain Transient Electromigration Analysis Using Circuit Theory #577, OPT: Optimal Proposal Transfer for Efficient Yield Optimization for Analog and SRAM Circuits #505, Spacing Cost-aware Optimal and Efficient Mixed-Cell-Height Detailed Placement for DFM Considerations #737, An Adversarial Active Sampling-based Data Augmentation Framework for AI-Assisted Lithography Modeling #434, PostPINN-EM: Fast Post-Voiding Electromigration Analysis Using Two-Stage Physics-Informed Neural Networks
Analog 1: **Advancements in Machine Learning and Modeling Techniques for RF Circuits and Power Grid Networks**	#413, FuNToM: Functional Modeling of RF Circuits Using a Neural Network Assisted Two-Port Analysis Method #886, One-Dimensional Deep Image Prior for Curve Fitting of S-Parameters from Electromagnetic Solvers #455, Accuracy-Preserving Reduction of Sparsified Reduced Power Grids with A Multilevel Node Aggregation Scheme #393, Multi-Task Evolutionary to PVT Knowledge Transfer for Analog Integrated Circuit Optimization

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Analog 2: **Novel frameworks and methodologies for optimizing analog/mixed-signal circuits**	#494, Multi-Product Optimization for 3D Heterogeneous Integration with D2W Bonding #307, Distributionally Robust Circuit Design Optimization under Variation Shifts #683, Practical Layout-Aware Analog/Mixed-Signal Design Automation with Bayesian Neural Networks #154, Design and Optimization of Low-Dropout Voltage Regulator Using Relational Graph Neural Network and Reinforcement Learning in Open-Source SKY130 Process
Bio 1: **Neuromorphic Wonders: Bridging Minds and Machines**	#621, ARMM: Adaptive Reliability Quantification Model of Microfluidic Designs and Its Graph-Transformer-Based Implementation #339, A Novel and Efficient Block-Based Programming for ReRAM-Based Neuromorphic Computing #745, Multi-Objective Architecture Search and Optimization for Heterogeneous Neuromorphic Architecture #402, Power-Aware Training for Energy-Efficient Printed Neuromorphic Circuits
Nano 1 **Emerging technologies for computation in memory**	#573, Lowering Latency of Embedded Memory by Exploiting In-Cell Victim Cache Hierarchy Based on Emerging Multi-Level Memory Devices #130, SEE-MCAM: A Scalable Multi-bit FeFET Content Addressable Memory for Energy Efficient Associative Search #421, Accelerating Polynomial Modular Multiplication with Crossbar-Based Compute-in-Memory #928, LIORAT: NN Layer I/O Range Training for Area/Energy-Efficient Low-Bit A/D Conversion System Design in Error-Tolerant Computation-in-Memory
NewComp 1: **Navigating the Future: A Voyage from Beyond CMOS to Beyond von Neumann**	#298, PBA: Percentile-Based Level Allocation for Multiple-Bits-Per-Cell RRAM #349, TL-nvSRAM-CIM: Ultra-High-Density Three-Level ReRAM-Assisted Computing-in-nvSRAM with DC-Power Free Restore and Ternary MAC Operations #1037, VECOM: Variation-Resilient Encoding and Offset Compensation Schemes for Reliable ReRAM-Based DNN Accelerator #131, Automated Synthesis for In-Memory Computing
NewComp 2: **Quantum Circuitry Unleashed: Innovations in Simulation, Synthesis, and Optimization**	#132, Full State Quantum Circuit Simulation Beyond Memory Limit #224, Optimizing LUT-based Quantum Circuit Synthesis using Relative Phase Boolean Operations #225, Optimal Layout Synthesis for Quantum Circuits as Classical Planning #352, Single-Qubit Gates Matter for Optimising Quantum Circuit Depth in Qubit Mapping
NewComp 3: **Frontiers in Quantum Computing: Novel Algorithms and Beyond**	#178, Effective and Efficient Qubit Mapper #446, Exact Logic Synthesis for Reversible Quantum-Flux-Parametron Logic #449, DLPlace: A Delay-Line Clocking-based Placement Framework for AQFP Circuits #487, QPulseLib: Accelerating the Pulse Generation of Quantum Circuit with Reusable Patterns

PROGRAM AT A GLANCE: Appendix B

SS 1 **AI for Sign-Off Showdown: Unveiling the Cost & Effect of Artificial Intelligence**	#42: Unleashing the Potential of Machine Learning: Harnessing the Dynamics of Supply Noise for Timing Sign-Off #52: Solving Fine-grained Static 3DIC Thermal with ML Thermal Solver Enhanced with Decay Curve Characterization #57: The Inevitability of AI Infusion into Design Closure and Signoff ##: Industry Trends for Power and Thermal Signoff in Advanced Nodes and Packaging
SS 2 **Towards Generative AI for EDA: Datasets, Benchmarks and Infrastructures**	#31: CircuitOps: An ML Infrastructure Enabling Generative AI for VLSI Circuit Optimization #35: VerilogEval: Evaluating Large Language Models for Verilog Code Generation #51: Verilog-to-PyG -- A Framework for Graph Learning and Augmentation on RTL Designs #55: Towards the Imagenets of ML4EDA
SS 3 **Sustainable AI Training at the Large and Tiny Scales**	##: Hardware-aware Sparsity: Accurate & Efficient Foundation Model Training ##: Federated Learning at Scale: Efficiency and Sustainability ##: DeepZero: Scaling Up Zeroth-order Optimization For Deep Model Training ##: Sustainable Training via Tensor Optimization
SS 4 **Next-Generation Computing Paradigm for Next-Generation (6G) Wireless**	#40: Accelerating Next-G Wireless Communications with FPGA-based AI Accelerators #41: MU-MIMO Detection Using Oscillator Ising Machines ##: In-Memory Computing for Belief Propagation-based Wireless DSP ##: NVidia Roadmap to AI-Infused 6G: Requirement, Architecture & Key Technologies
SS 5 **Frontiers in Edge AI: Technology, Algorithms, and Emerging Trends**	#30: Towards the Efficiency, Heterogeneity, and Robustness of Edge AI #34: Ultra-Efficient Edge AI using FeFET-based Monolithic 3D Integration #36: Algorithm/Hardware Codesign for Few-Shot Learning at the Edge #44: Hyperdimensional Computing for Resilient Edge Learning ##: Interpretable and Robust Reasoning on Edge
Tutorial 1	#33: Introduction to Hybrid Quantum-Classical Programming Using C++ Quantum Extension

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SS 7 **CAD Contest at ICCAD**	#48: Overview of 2023 CAD Contest at ICCAD #39: CAD Contest Problem A: Multi-bit Large-scale Boolean Matching #32: CAD Contest Problem B: 3D Placement with Macros #53: CAD Contest Problem C: Static IR Drop Estimation Using Machine Learning #56: IEEE CEDA DATC: Emerging Foundations in IC Physical Design and ML-CAD Research
SS 8 **Accelerating EDA Algorithms with Heterogeneous Parallelism**	#43: Programming Dynamic Task Parallelism for Heterogeneous EDA Algorithms #46: Accelerating Routability and Timing Optimization with Open-Source AI4EDA Dataset CircuitNet and Heterogeneous Platforms ##: Macro Placement with GPU-accelerated Placer and Automated Parameter Tuning ##: Heterogenous Acceleration for Design Rule Checking
Tutorial 2	#37: RapidWright: Unleashing the Full Power of FPGA Technology with Domain-Specific Tooling
SS 10 **In-Sensor AI Computing Towards Next-Generation Autonomous Edge Intelligence**	##: Neural Sensors: AI driven In-Pixel Compute for Compressed Readout Bandwidth ##: On-Silicon In-Sensor Computing ##: The Path and Challenges to Bionic Vision as the Next "Moore's Law" Won't Be Defined by Transistor Density #38: Learned In-Sensor Visual Computing: From Compression to Eventification #50: In-Sensor Radio Frequency Computing for Energy-Efficient Intelligent Radar
SS 11 **From Arithmetic Components to Side Channel Attacks: a Deep Dive in Post Quantum Hardware**	#45: Instruction Set Extensions for Post-Quantum Cryptography #47: Machine Learning based Blind Side-Channel Attacks on PQC-based KEMs - A Case Study of Kyber KEM #49: A Scalable Hardware/Software Co-design Approach for Efficient Polynomial Multiplication #54: Dilithium Hardware-Accelerated Application using OpenCL-based High-Level Synthesis ##: A Scalable Hardware/Software Co-design Approach for Efficient Polynomial Multiplication

PROGRAM AT A GLANCE

IEEE/ACM 2023 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN
ICCAD
42nd Edition

Thursday, November 2, 2023

Time	Sculptor	Artisan	Salon I	Salon II	Atelier I & II
07:30	Breakfast (3rd Floor Foyer)				
08:00	Fast ML for Science	System Level Interconnect Path Finding	VLSI Education Community	Zero Trust Hardware Architectures	SUSHI
08:30					
09:00					
09:30					
10:00	Coffee Break (3rd Floor Foyer)				
10:30	Fast ML for Science	System Level Interconnect Path Finding	VLSI Education Community	Zero Trust Hardware Architectures	SUSHI
11:00					
11:30					
12:00	Lunch (3rd Floor Foyer)				
12:30					
13:00	Fast ML for Science	System Level Interconnect Path Finding		Zero Trust Hardware Architectures	SUSHI
13:30					
14:00					
14:30					
15:00					
15:30	Coffee Break (3rd Floor Foyer)				
16:00	Fast ML for Science	System Level Interconnect Path Finding		Zero Trust Hardware Architectures	SUSHI
16:30					
17:00					