ICMC 2026

International Compact Modeling Conference

July 30 - July 31, 2026 || The Queen Mary || Long Beach, CA

INTERNATIONAL COMPACT MODELING CONFERENCE

CONFERENCE PROGRAM

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Welcome Message from the General Chair

On behalf of the organizing committee, welcome to the International Compact Modeling Conference (ICMC) 2026 in Long Beach, California.

We are pleased to host the second edition of ICMC aboard the historic Queen Mary. Building on the success of the inaugural conference in 2025, our goal this year is to continue growing ICMC as a focused venue for compact modeling and its expanding impact on the semiconductor industry. ICMC was created to provide a dedicated forum for the compact modeling community, as there are very few conferences centered specifically on compact device models, their development, standardization, implementation, validation, and application. By bringing together model developers, circuit designers, semiconductor technologists, EDA professionals, and researchers from academia, industry, and government laboratories, ICMC aims to help fill that gap.

The 2026 conference continues under the theme “Enhancing Collaboration in Modeling with the Semiconductor Industry.” This year, ICMC especially encourages contributions in several timely and important areas, including electrostatic discharge (ESD) modeling for protection design, reliability and aging-aware compact models and simulation techniques, and the use of AI or machine learning for model development, parameter extraction, and circuit simulation efficiency. The conference also covers a broad range of topics in compact modeling, including the application of device models, device model development, model enhancements and implementations, and emerging devices.

This year’s technical program includes 3 keynote speakers, 7 invited speakers, 28 technical talks, 12 posters and a panel session. The program reflects both the depth and diversity of current modeling research and practice, ranging from model calibration and validation methodologies to reliability, RF, high-voltage, cryogenic, and emerging device applications.

I would like to extend special thanks to Si2, under the leadership of CEO Rob Aslett, for providing financial and organizational support for the conference. I wish to recognize Leigh Anne Clevenger and Sheena Taylor for their support and help in publicity and logistics, Peter Lee in his role as CMC Chair for his continued leadership and guidance, and Alexandria Heverly and the Conference Catalysts team for their professional assistance in organizing and executing the conference.

We are grateful to our technical sponsors, the IEEE Electron Devices Society (EDS) and the IEEE Microwave Theory and Technology Society (MTT-S), and to Shu Ikeda, EDS conference committee chair, Valentina Palazzi, MTT-S conference committee chair, and Yogesh Chauhan and Bernard Lim from EDS for their support of the conference.

Many thanks to our industry sponsors Cadence Design Systems, Keysight Technologies, Micron Technology, Qualcomm, Sandia National Laboratories, Siemens, Synopsys, and TCMC, and our media sponsors, SemiWiki and Semiconductor Digest, for helping us promote and strengthen the conference.

I would also like to thank the members of the organizing team for their work and commitment to putting this conference together. In particular I would like to recognize Harshit Agarwal (Vice Chair), Gert-Jan Smit (Technical Program Chair), Girish Pahwa (Technical Program Vice-Chair), Wladek Grabinski (Publicity Committee Chair), and organizing committee members Thomas Bédécarrats and Fahad Usmani for their contributions. Thank you to all of our paper reviewers, whose efforts were essential in maintaining the quality of the technical program.

Finally, thank you to all the authors, speakers, and attendees for being part of ICMC 2026. We hope the program provides comprehensive coverage of compact modeling topics and gives attendees the opportunity to benefit from the full breadth of the conference, while the Queen Mary venue offers a unique and memorable setting for technical exchange and professional networking.

Shahed Reza
General Chair, ICMC 2026

Thank You to Our Conference Sponsors

The Silicon Integration Initiative (Si2) is a 501(c)(6) not-for-profit, membership-based organization funded by our member companies. Si2 provides collaborative technology and services which enable higher levels of semiconductor design integration leading to industry-accepted standards. Si2 provides a unique, collaborative environment and access to shared solutions for users and suppliers from corporations, institutions and academia. Si2 solutions are co-developed in a way that permits innovation while guaranteeing compatibility with trusted standards. Some members have leadership roles and participate broadly across Si2. Some members focus on specific areas of interest. Others join to primarily gain access to Si2 solutions. All are welcome.

The Compact Model Coalition (CMC) is composed of industry and academic leaders who select, develop, and standardize SPICE simulation models in a way that assures accuracy with target applications. The CMC funds research and collaborative groups to make semiconductor device model standardization a reality. Proven standards have been evolving for decades and new standards continue to be added, providing tremendous savings to the industry by the CMC taking responsibility for supervision of the model standardization, maintenance, and validation.

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Keynote Presentations

Chenming Hu
TSMC Distinguished Chair Professor Emeritus, University of California, Berkeley, USA

BSIM, FinFET, and Open Innovation
Open-source research like the CMC standard codes is less celebrated than the commercial successes of closed innovations. Open innovation, nonetheless, is an important driver of digital technologies. Prof. Don Pederson, starting with his SPICE, built a culture of open-sourcing the university's research at UC Berkeley. That open EDA research tradition continues with BSIM and the Berkeley RISC. It has also influenced the successful spread of FinFET. A good balance between open and closed innovations is important to the advancement and safety of technology.

Yuan Taur
University of California, San Diego, USA

Physical Insights Beyond the Textbook Modeling of MOSFETs and p-n Junctions
This talk brings out the shortfalls of conventional textbook modeling of p-n junctions and MOSFETs, then goes over more elaborate models that can deal with those problems. For p-n junctions, the conventional depletion approximation only works for forward bias voltages below the built-in potential. For MOSFETs, the commonly practiced gradual channel approximation (GCA) fails in the velocity saturation region. It is shown that the conventional terms of pinch-off and channel length modulation are misleading. A non-GCA MOSFET model that takes the potential curvature in the source-drain direction into account is described. It generates continuous current-voltage solutions from the triode region into the velocity saturation region with finite output conductance. Lastly, the concept of “threshold voltage” is investigated by examining the Qi-Vgs characteristics of an undoped double-gate MOSFET as a function of temperature. An unambiguously defined threshold voltage emerges when the electron thermal energy is diminished.

Keynote Presentations (Continued)

Elyse Rosenbaum
University of Illinois Urbana-Champaign, USA

Measurement Challenges Impeding the Verification of ESD Compact Model Accuracy and Generalizability

At this point in history, most ESD specialists believe that the physics underlying ESD device behavior are understood and can be expressed in the form of a compact model. Optimizing and validating those models remains a challenge and will be the main focus of this presentation. However, for the benefit of non-ESD specialists, the talk will start with a brief introduction to CMOS ESD protection devices and their behavior.

Invited Presentations

James Victory
Onsemi, USA

Modeling and Simulation Challenges in Modern Power Discrete Semiconductor Technologies

Modern discrete power devices such as SiC MOSFETs presents significant modeling and simulation challenges, motivating the need for accurate, physics-based SPICE models to achieve first-time-right system design. This paper outlines a SPICE-agnostic approach for implementing nonlinear electrical behavior, scalable geometry equations, and correct thermal-impedance modelling suitable for discrete devices and power modules. A unified characterization flow is presented that incorporates pulsed I–V, short-circuit waveforms, and detailed parasitic extraction to accurately predict switching performance and energy losses. The resulting methodology supports reliable electrical-thermal simulation and enables robust virtual prototyping for next-generation power-electronics applications.

Gilson Wirth
UFRGS, Porto Alegre, Brazil

Modeling of Low-Frequency Noise and BTI in Electron Devices

Charge capture and emission by defects (traps) close to the conduction channel is a major source of noise and aging in modern electron devices. A comprehensive physics-based modeling and simulation approach for Bias Temperature Instability (BTI), Random Telegraph Noise (RTN) and low-frequency (1/f) noise is reviewed, discussed and summarized. It allows for the derivation of analytical formulations for 1/f noise (frequency domain), RTN (time domain) and BTI (aging) using a single modeling framework, where model parameters are the same in frequency and time domain. Operation under cyclo-stationary conditions is also modeled.

Time domain analysis is relevant for the analysis of digital and mixed-signal circuits. In digital circuits, the RTN chronological statistics, especially trap occupancy switching, have direct impacts on circuit performance and reliability, as degradations like jitter of signals happen if a trap switches state.

Noise and BTI levels can vary by several orders of magnitude in deeply scaled devices, making variability among devices a major concern. To ensure proper circuit design in this scenario, it is necessary to identify the fundamental mechanisms responsible for the variability in noise and BTI. We discuss how the statistics of RTN and BTI scale with device area and show how physical parameters can be extracted using the model.

Invited Speakers (Continued)

Chien-Ting Tung
Synopsys Inc., USA

Application of AI and ML in the Compact Modeling Domain

This review surveys recent advances in the application of artificial intelligence (AI) and machine learning (ML) within the compact modeling domain for integrated circuits. Neural network (NN) compact models, including pure NN, compensation NN, and knowledge-based NN, are briefly discussed, with emphasis on the recently developed physics-enhanced neural networks (PENN). PENN incorporates physics into its NN formulation, enabling modeling of process variation (PV) and local layout effects (LLE) through physical model parameters in preprocessing and postprocessing. The review also covers ML-assisted model parameter (MP) extraction, highlighting multi-stage and reinforcement learning strategies for scalability and adaptability. Transient circuit simulation, emerging memory, and aging models are addressed using recurrent neural networks (RNN), while variation and layout effects are explored through weight perturbations and variational autoencoders. As device complexity increases, the integration of AI and ML is expected to play a critical role in advancing reliable simulation and innovation in compact modeling.

Transient circuit simulation, emerging memory, and aging models are addressed using recurrent neural networks (RNN), while variation and layout effects are explored through weight perturbations and variational autoencoders. As device complexity increases, the integration of AI and ML is expected to play a critical role in advancing reliable simulation and innovation in compact modeling.

Michael Stockinger
NXP Semiconductors, USA

On-Chip ESD Protection Design Optimization Using ESD Device Compact Models

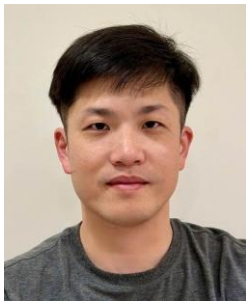
Accurate ESD compact models are essential for designing robust on-chip protection in advanced CMOS technologies. This work presents three case studies showing how calibrated ESD models enable reliable prediction of stress voltages and guide optimization of ESD protection networks. The results demonstrate that standardized, measurement-based ESD models are critical for achieving required ESD performance levels in modern IC designs.

Invited Speakers (Continued)

Darsen Lu
Dept. of Electrical Engineering, National Cheng Kung University, Tainan, Taiwan

Ferroelectric Memory Devices Compact Modeling and Applications

In this invited paper, we discuss several compact modeling approaches for ferroelectric memory devices. A novel sub-circuit extends the single-domain Landau-Khalatnikov equation to consider ferroelectric capacitors with multiple domains and can explain the special transient waveform we have measured. To model FE FETs as synaptic device in the context of online neural network (NN) training, on the other hand, simple BSIM-based expressions for Id-Vgs for various programmed states is adopted. NN inference accuracy as function of temperature, bias voltage, in the presence of device variation, and over time after retention degradation, are all captured with the model. Finally, the nucleation-limited switching (NLS) model captures minor loops and frequency dependence better in a physical manner, although the simulation time is found to be significantly longer. With the NLS model we demonstrated the simulation of recall operation for non-volatile SRAM (NV-SRAM). A special recall scheme, where the voltage of the plate-line is raised before the supply voltage is, allows for better design margin during recall operation, and reduces area requirements for NV-SRAM.



Meng-Lin Lu
Taiwan Semiconductor Manufacturing Company, Taiwan

Applications of Machine Learning Techniques in the Compact Modeling Platform

The semiconductor industry increasingly relies on Machine Learning (ML) techniques to drive advancements in efficiency and capability. This article introduces a Compensation-based MOSFET model framework, distinguished by its extendibility based on existing physics-based model equations. In addition to this core MOSFET model, we will present Convolutional-based layout extraction methodologies tailored for intricate multi-physics simulations. A key focus of this work will also be the demonstrated benefits of these ML-oriented solutions within the design sign-off flow. The evolution of SPICE platforms is significantly aided by the TSMC Model Interface (TMI/TMI-RC), which has pioneered close collaborations with Electronic Design Automation (EDA) partners, contributing to the progress of the entire semiconductor community.

Invited Speakers (Continued)

Lorenzo Peri
Quantum Motion, United Kingdom

Compact Quantum Dot Models for Hybrid Microwave Circuits and Quantum Information Processing

Scalable solid-state quantum computation demands integration of quantum system with digital and analog electronics. This needs to be achieved at deep-cryogenic temperatures (≤10K) and within constrained power and noise budgets to protect the quantum information from decoherence. Leveraging quantum phenomena may help alleviate such challenges, enabling ultra-low-power hybrid quantum-classical microwave circuits for qubit control and readout. We presents novel compact modeling of quantum systems that recasts the quantum dynamics into coupled differential equations compatible with the standard modified nodal analysis used by electrical circuit simulators, and present the implementation of qubit models in Verilog-A demonstrating accurate representation of coherent quantum phenomena. This work paves the way for the use of standard EDA tools in the field of quantum technologies to simulate the behavior of pure quantum and quantum-classical hybrid circuits.

Program Grid – Thursday, July 30th

Time	Session
8:30 – 8:45	Day 1 Welcome *(Queens Salon)*
8:45 – 9:25	[Keynote] BSIM, FinFET, and Open Innovation by Chenming Hu *(Queens Salon)*
9:25 – 10:25	Advances in Compact Modeling *(Queens Salon)*
10:25 – 10:45	Coffee Break *(Royal Salon & Kings View Room)*
10:45 – 12:10	Ferroelectric and other Nonvolatile Memories *(Queens Salon)*
12:10 – 13:20	Lunch Served *(Royal Salon & Kings View Room)*
13:20 – 14:00	[Keynote] Physical Insights Beyond the Textbook Modeling of MOSFETs and p-n Junctions by Yuan Taur *(Queens Salon)*
14:00 – 15:05	Emerging Devices and Technologies *(Queens Salon)*
15:05 – 15:25	Coffee Break *(Royal Salon & Kings View Room)*
15:25 – 16:30	Wide Bandgap Material Device Models *(Queens Salon)*
16:30 – 17:00	Poster Introductions *(Queens Salon)*
17:00	Poster Session & Reception – Appetizers & Beverages Served *(Verandah Grill/Deck)*

Program Grid – Friday, July 31st

Time	Session
8:30 – 8:40	Day 2 Welcome *(Queens Salon)*
8:40 – 9:20	[Keynote] Measurement Challenges Impeding the Verification of ESD Compact Model Accuracy and Generalizability Prof. Elyse Rosenbaum *(Queens Salon)*
9:20 – 10:05	ESD Protections Modeling *(Queens Salon)*
10:05 – 10:25	Coffee Break *(Royal Salon & Kings View Room)*
10:25 – 11:55	Machine Learning and Artificial Intelligence in Compact Modeling *(Queens Salon)*
11:55 – 12:55	Lunch Served *(Royal Salon & Kings View Room)*
12:55 – 13:55	Panel Session: Machine Learning for Compact Modeling: Promises, Pitfalls, and Paths to Industry Adoption Panelists: Chien-Ting Tung, Kiran Gullapalli, Hyunbo Cho, Gajanan Dessai *(Queens Salon)*
13:55 – 14:40	Modeling of Noise and Traps *(Queens Salon)*
14:40 – 15:00	Coffee Break *(Royal Salon & Kings View Room)*
15:00 – 16:20	Devices at Cryogenic Temperatures *(Queens Salon)*
16:20	Closing Ceremony & Awards *(Queens Salon)*

Technical Program – Thursday, July 30th

08:30 – 09:25
Day 1 Conference Opening & Keynote Presentation
Room: Queens Salon
Session Chair: Gert-Jan Smit, NXP Semiconductors

08:30 – 8:45
Day 1 Conference Opening

08:45 - 09:25
[Keynote] **BSIM, FinFET, and Open Innovation**
Chenming Hu
TSMC Distinguished Chair Professor Emeritus, University of California, Berkeley

09:25 - 10:25
Session 1: Advances in Compact Modeling
Room: Queens Salon
Session Chair: Gert-Jan Smit, NXP Semiconductors

09:25 - 09:45
[1.1] Modeling of Contact-To-Gate Capacitance in Gate-All-Around FET
Ning Lu[1], Richard Wachnik[2]
[1]IBM, Essex Junction, Vermont, USA. [2]IBM, Poughkeepsie, New York, USA

09:45 - 10:05
[1.2] Compact Modeling of Base Current High Injection Effect in SiGe HBTs
Yiao Li[1], Guofu Niu[1], Marnix Willemsen[2], Andries Scholten[2]
[1]Auburn University, Auburn, USA. [2]NXP, Eindhoven, Netherlands

10:05 - 10:25
[1.3] Why Compact Models Need a Proper Branch Topology and Node/Branch Scaling for Convergence
Alexander Schade, Stefan Jahn, Klaus-Willi Pieper, Michael Asam
Infineon Technologies AG, Neubiberg, Germany

10:25 - 10:45
Coffee Break
Room: Royal Salon & Kings View Room

10:45 - 12:10
Session 2: Ferroelectric and other Nonvolatile Memories
Room: Queens Salon
Session Chair: Harshit Agarwal, ITT Jodhpur

10:45 - 11:10

[2.1 INVITED] **Ferroelectric Memory Devices Compact Modeling and Applications**

Darsen Lu
National Cheng Kung University, Tainan City, Taiwan

11:10 - 11:30

[2.2] Validation of a Variation-Aware Physics-Based RRAM Compact Model Using 1T1R Array Data

Tommaso Zanotti[1], Andrea Baroni[2], Tommaso Rizzi[2], Emilio Pérez-Bosch Quesada[2], Keerthi Dorai Swamy Reddy[2], Eduardo Pérez[2,3], Christian Wenger[2,3], Paolo Pavan[1], Francesco Maria Puglisi[1]
[1]University of Modena and Reggio Emilia, Modena, Italy. [2]IHP – Leibniz Institute for High Performance Microelectronics, Frankfurt (Oder), Germany. [3]BTU Cottbus-Senftenberg, Cottbus, Germany

11:10 - 11:30

[2.3] Using UMEM-FE for Ferroelectric Circuit Simulation

Chien-Ting Tung
Synopsys, Sunnyvale, USA

11:50 - 12:10

[2.4] Physics-informed AI Accelerated Retention Analysis of Ferroelectric Vertical NAND: From Day-Scale TCAD to Second-Scale Surrogate Model

Gyujun Jeong[1], Sungwon Cho[1], Minji Shon[1], Namhoon Kim[1], Woohyun Hwang[2], Kwangyou Seo[2], Suhwan Lim[2], Wanki Kim[2], Daewon Ha[2], Prasanna Venkatesan[3], Kihang Youn[3], Ram Cherukuri[3], Yiyi Wang[3], Suman Datta[1], Asif Khan[1], Shimeng Yu[1]
[1]Georgia Institute of Technology, Atlanta, USA. [2]Samsung Electronics, Hwaseong, Korea, Republic of. [3]NVIDIA, Santa Clara, USA

12:10 - 13:20
Lunch Served
Room: Royal Salon & Kings View Room

Technical Program – Thursday, July 30th

13:20 - 14:00
Keynote Presentation
Room: Queens Salon
Session Chair: Girish Pahwa, NYCU Taiwan

13:20 - 14:00
[Keynote] Physical Insights Beyond the Textbook Modeling of MOSFETs and p-n Junctions
Yuan Taur
University of California, San Diego

14:00 - 15:05
Session 3: Emerging Devices and Technologies
Room: Queens Salon
Session Chair: Girish Pahwa, NYCU Taiwan

14:00 – 14:25
[3.1 INVITED] Compact Quantum Dot Models For Hybrid Microwave Circuits And Quantum Information Processing
Lorenzo Peri[1], Alberto Gomez-Saiz[1,2], M. Fernando Gonzalez-Zalba[1,3,4]
[1]Quantum Motion, London, United Kingdom. [2]Imperial College, London, United Kingdom. [3]CIC nanoGUNE BRTA, Donostia-San Sebastian, Spain. [4]IKERBASQUE, Bilbao, Spain

14:25 - 14:45
[3.2] Compact Time-Domain Modeling of Parameterized Frequency-Dependent Photonic Components in Verilog-A
Zhengxing Zhang, Weijia Li, Yihao Cui, Xu Wang
Cadence Design Systems, Port Moody, Canada

14:45 - 15:05
3.3 Bias-dependent capacitance compact model of an Organic Electrochemical Transistor
Ermias Telahun Teka[1], Laura Teuerle[2], Tommy Meier[2], Olga Morozova[2], Hans Kleemann[2], Benjamin Iñiguez[1], [1]Universitat Rovira i Virgili, Tarragona, Spain. [2]Technische Universität Dresden, Dresden, Germany

15:05 - 15:25
Coffee Break
Room: Royal Salon & Kings View Room

Technical Program – Thursday, July 30th

15:25 - 16:30
Session 4: Wide Bandgap Material Device Models
Room: Queens Salon
Session Chair: Guofu Niu, Auburn University, Auburn, USA

15:25 - 15:50

[4.1 INVITED] Modeling and Simulation Challenges in Modern Power Discrete Semiconductor Technologies

James Victory[1], Matej Klement[2], Dan Zurek[2], Kan Jia[3], Jiri Lehocky[2], Canzhong He[4], Yunpeng Xiao[3], Jaume Roig Guitart[5]

[1]onsemi, Sunnyvale, USA. [2]onsemi, Brno, Czech Republic. [3]onsemi, Shanghai, China. [4]onsemi, Mountain Top, USA. [5]onsemi, Mechelen, Belgium

15:50 - 16:10

[4.2] Accurate High-Temperature Modeling of GaN HEMTs Within ASM-HEMT Framework

Mir Mohammad Shayoub[1], Siddharth Thakur[1], Shivendra Singh Parihar[2], Aleksei Vasilev[3], Yogesh Singh Chauhan[1]

[1]Indian Institute of Technology Kanpur, Kanpur, India. [2]University of California, Berkeley, USA. [3]INGAIN Technologies Pvt. Ltd., Bangalore, India

16:10 - 16:30

[4.3] Nonlinear Passive Elements for Compact Modeling of GIT Charge Trapping Including Hole Injection Effects

Fadi Zaki, Volker Kubrak, Hannes Maier-Flaig, Klaus-Willi Pieper, Miguel Martins, Klaus Oettinger

Infineon Technologies AG, Munich, Germany

Technical Program – Thursday, July 30th

16:30 - 17:00
Poster Intros (One-minute/one-slide presentation of each poster)
Room: Queens Salon
Session Chair: Jason Verley, Sandia National Laboratories, USA

17:00 – 19:00
Poster Session & Reception - *Appetizers & Beverages Served*
Room: Verandah Grill/Deck

P1 Strategy to Enable Accurate and Efficient Aging Models for BJTs and MOSFETs
Jung-Suk Goo[1], Oscar Huerta Gonzalez[2], Maria Toledano Luque[2], Wafa Arfaoui[3], Germain Bossu[3], Anil Allampalli[4], Priyansh Kasyap[4], Dattatreya Prabhu Rachakonda[4], Adam DiVergilio[2], Dimitrios P. Ioannou[2], Mohamed Mahmoud Ismail[5], Ahmed Abo-Elhadid[5]
[1]GlobalFoundries, Santa Clara, USA. [2]GlobalFoundries, Malta, USA. [3]GlobalFoundries, Dresden, Germany. [4]GlobalFoundries, Bangalore, India. [5]Siemens EDA, Cairo, Egypt

P3 Impact of Distributed Modeling of The External Base-Collector Region On Sige HBT Device Characteristics
Guangsheng Liang[1], Michael Schröter[1,2]
[1]Chair for Electron Devices and Integrated Circuits (CEDIC), TU Dresden, Dresden, Germany. [2]Advanced Device Modeling Enterprises, Escondido, USA

P4 Enabling Circuit Simulations with Compact Gray Box Radiation Models via Xyce-PyMi
Paul Kuberry
Sandia National Laboratories, Albuquerque, USA

P5 Three Terminal CMOM Model with Symmetry, Reciprocity and Charge Conservation
Chuan Xu[1], Sergey Cherepko[2], William Liu[1]
[1]Analog Devices, Inc., Beaverton, USA. [2]Analog Devices, Inc., Wilmington, USA

P6 Improving NN-Assisted Compact Models with Control Variate
Anamika Singh[1], Srishti Parandiyal[1], Kumar Sheelvardhan[1], M. Ehteshamuddin[2], Samrat Roy[3], Abhishek Somani[3], Sourajeet Roy[1], Avirup Dasgupta[1]
[1]INDIAN INSTITUTE OF TECHNOLOGY, ROORKEE, India. [2]Intel Corporation, Bengaluru, India. [3]Siemens EDA, Gurugram, India

Technical Program – Thursday, July 30th

P8 Automated Parameter Extraction and Hybrid Artificial Neural NetworkIntegration for GaAs pHEMT Modeling

Yiao Li[1], Mohammed Ehteshamuddin[2], Fahad Usmani[3], Song Lin[2], Shaoli Lyu[4], Roberto Tinti[5], Long Ma[1]

[1]Keysight Technologies, Beijing, China. [2]Analog Devices, Wilmington, USA. [3]Keysight Technologies, Santa Clara, USA. [4]Keysight Technologies, Houston, USA. [5]Keysight Technologies, Calabasas, USA

P9 A 4 K-393 K SAR ADC with Automatic Vth Compensation in 22 FDX Technology

Yiming Fan[1], Anni Zhang[1], Ergen Tao[1], Harshil Goyal[1], Guofu Niu[1], Michael Hamilton[1], Fa Foster Dai[1], John D. Cressler[2]

[1]Auburn University, Auburn, AL, USA. [2]Georgia Tech, Atlanta, GA, USA

P10 Compact Modeling and Analysis of Subthreshold Anomalies in Organic Thin Film Transistors

Amer Zaibi[1], Antonio Cerdeira[1], Magali Estrada[1], Fetene Mulugeta[1], Sami El Nakouzi[2], Laurie E Calvet[2], Mohamed Benwadih[3], Lina Kadura[3], Benjamin Iniguez[1]

[1]Rovira I Virgili, Tarragona, Spain. [2]CNRS ecole polytechnique, Paris, France. [3]CEA,LITEN, Grenoble, France

P11 Compact Circuit Models for EM Effects Based on Statistical Decomposition of System Dynamics

Teddy Meissner[1,2], Joshua Hanson[2], Joshua Young[2], Pavel Bochev[2]

[1]University of Arizona, Tucson, USA. [2]Sandia National Laboratories, Albuquerque, USA

P12 Virtual-Source-Based Cryogenic FET Model

Hazem Elgabra, Dylan Ma, Rubaya Absar, Francois Sfigakis, Jonathan Baugh, Lan Wei

University of Waterloo, Waterloo, Canada

Technical Program – Friday, July 31st

08:30 – 9:20
Day 2 Conference Opening & Keynote Presentation
Room: Queens Salon
Session Chair: Thomas Bédecerrats, CEA-Leti, France

08:30 – 8:40
Day 2 Conference Opening

08:40 - 09:20
[Keynote] **Measurement Challenges Impeding the Verification of ESD Compact Model Accuracy and Generalizability**
Elyse Rosenbaum,

09:20 - 10:05
Session 5: ESD Protections Modeling
Room: Queens Salon
Session Chair: Thomas Bédecerrats, CEA-Leti, France

09:20 – 09:45
[5.1 INVITED] **On-chip ESD Protection Design Optimization Using ESD Device Compact Models**
Michael Stockinger
NXP Semiconductors, Austin, USA

09:45 - 10:05
[5.2] Comprehensive ESDFET Compact Model Including Symmetric and Secondary Snapback Phenomena
Anant Singhal[1], Girish Pahwa[2], Harshit Agarwal[1]
[1]Indian Institute of Technology Jodhpur, Jodhpur, India. [2]National Yang Ming Chiao Tung University, Hsinchu, Taiwan

10:05 – 10:25
Coffee Break
Room: Royal Salon & Kings View Room

Technical Program – Friday, July 31st

10:25 - 11:55
Session 6: Machine Learning and Artificial Intelligence in Compact Modeling
Room: Queens Salon
Session Chair: Shahed Reza, Sandia National Laboratories

10:25 – 10:50

[6.1 INVITED] Applications of Machine Learning Techniques in the Compact Modeling Platform

Meng-Lin Lu, Cheng Hsiao, Jui-Hsuan Chang, Switch Su, Jyun-Yan Kuo, Gary Lee, Kasa Huang, Jim Liang, Yi-Hung Tsai, Orion Yu, Wen-Che Chang, Eugene Chen, Guan-Ming Huang, Chien-Ming Hung, Jin-Yu Lin, CHAO-HSUN Liu, Ke-Wei Su, Chung-Kai Lin
Taiwan Semiconductor Manufacturing Company, HsinChu, Taiwan

10:50 - 11:10

[6.2] Neural Compact Model Retargeting Using Pseudo Labeling for Accurate I-V Curve Prediction

Jeonghwan Kim, Yongjeong Lee, Youngbin Lee, Jeongyeol Kim, Jungyun Choi
Samsung Electronics Co. Ltd., Hwasung-si, Korea

11:10 - 11:35

[6.3 INVITED] Application of AI and ML in the Compact Modeling Domain

Chien-Ting Tung[1], Jen-Hao Chen[2], Chenming Hu[2]
[1]Synopsys, Sunnyvale, USA. [2]UC Berkeley, Berkeley, USA

11:35 - 11:55

[6.4] Physics-Informed Neural Networks for Predicting Characteristics of β-Ga_2O_3 based Devices

Tasnia Jahan, Kexin Li
Arizona State University, Tempe, USA

11:55 - 12:55
Lunch Served
Room: Royal Salon & Kings View Room

Technical Program – Friday, July 31st

12:55 - 13:55
Panel Session
Room: Queens Salon
Session Chair: Girish Pahwa, NYCU Taiwan

12:55 – 13:55
[Panel Session] Machine Learning for Compact Modeling: Promises, Pitfalls, and Paths to Industry Adoption
Panelists: Chien-Ting Tung, Kiran Gullapalli, Hyunbo Cho, and Gajanan Dessai

13:55 - 14:40
Session 7: Modeling of Noise and Traps
Room: Queens Salon
Session Chair: Patrick Scheer, STMicroelectronics, Crolles, France

13:55 – 14:20
[7.1 INVITED] Modeling of Low-Frequency Noise and BTI in Electron Devices
Gilson Wirth[1], Mauricio Banaszeski da Silva[2], Thiago Hanna Both[3], Roberto da Silva[1]
[1]UFRGS, Porto Alegre, Brazil. [2]UFSM, Santa Maria, Brazil. [3]NXP Semiconductors, Eindhoven, Netherlands

14:20 - 14:40
[7.2] Bridging Time and Frequency Domains: A Unified Trap-Based RTN Modeling Framework
Yu Li[1], Zixuan Sun[2], Lining Zhang[1], Runsheng Wang[2]
[1]Peking University Shenzhen Graduate School, Shenzhen, China. [2]Peking University, Beijing, China

Technical Program – Friday, July 31st

14:40 - 15:00
Coffee Break
Room: Royal Salon & Kings View Room

15:00 - 16:20
Session 8: Devices at Cryogenic Temperatures
Room: Queens Salon
Session Chair: Klaus-Willi Pieper, Infineon Technologies AG, Munich, Germany

15:00 - 15:20

[8.1] Cryogenic Modeling of Bulk LDMOS Devices: A Physics-Based BSIM-BULK Compact Model Extension

Luis Pöller[1,2], Mingchun Tang[2], Klaus-Willi Pieper[2], Qing-Tai Zhao[3], Amelie Hagelauer[1,4]
[1]Technical University of Munich, Munich, Germany. [2]Infineon Technologies AG, Munich, Germany. [3]Forschungszentrum Jülich, Jülich, Germany. [4]Fraunhofer EMFT, Munich, Germany

15:20 - 15:40

[8.2] Enhancing L-UTSOI Compact Model Accuracy with an Asymmetric Mobility correction for Cryogenic SPICE simulations

Miltiadis Alepidis[1], Thomas Bédécarrats[1], Aurélie Bajolet[1], Benjamin Dormieu[2], Patrick Scheer[2], Sébastien Martinie[1]
[1]Univ. Grenoble Alpes, CEA, Leti, Grenoble, France. [2]STMicroelectronics, Crolles, France

15:40 - 16:00

[8.3] Surface potential equation for asymmetric double gate MOSFETs operating at Cryogenic Temperature

Thomas Bédécarrats, Sébastien Martinie
Univ. Grenoble Alpes, CEA, Leti, Grenoble, France

16:00 - 16:20

[8.4] Cryogenic Extensions to Mextram for SiGe HBTs Down to 19 K

Anni Zhang[1], Guofu Niu[1], Priyotous Tirtha[1], Andries Scholten[2], Marnix Willemsen[2]
[1]Auburn University, Auburn, USA. [2]NXP Semiconductors, Eindhoven, Netherlands

16:20 - 17:00
Closing Ceremony & Feedback
Room: Queens Salon