ICMC 2026

International Compact Modeling Conference

July 30 - July 31, 2026 || The Queen Mary || Long Beach, CA

The Compact Model Coalition (CMC) brings academia and industry partners together in the development and standardization of compact models for semiconductor devices. For more than 30 years, the CMC has been instrumental in creating standardized and verified models for designers to use in their increasingly complex circuits for SPICE simulation. The CMC is organizing the second edition of the International Compact Modeling Conference, cosponsored by IEEE EDS. It will focus uniquely on compact device models, their development, and broad application in the semiconductor industry. You are invited to participate in the evolution of these models, guiding model development to help circuit designers achieve the best circuit performance possible, and enabling foundries to leverage the strength of their device fabrication to the full extent. Join world experts in design, process technology, and model development for a two-day in-person event to discuss state-of-the-art semiconductor device modeling, offering a rare opportunity to present and learn about this core element of circuit design and how to get the most from these global collaborations.

HIGHLIGHTED THEMES FOR ICMC 2026

This year, ICMC especially encourages submissions in the following domains:

- Electrostatic Discharge (ESD) modeling for protection design
  - Modeling of parasitic BJT activation, snapback behavior, ESD stress and breakdown, transient response, failure prediction, etc.
- Reliability and aging-aware compact models and simulation techniques
  - for degradation mechanisms such as Bias Temperature Instability (BTI), Hot Carrier Degradation (HCI), Time Dependent Dielectric Breakdown (TDDB)
  - self-heating and circuit reliability prediction
- AI or Machine Learning for model development, parameter extraction, circuit simulation efficiency, etc.

GENERAL TOPICS

We are also seeking submissions in the following domains.

Application of Device Models

- Innovative application of CMC standard device models
- Designer's perspective: best practices, novel use, and benefits of standard device models to improve circuit design and system performance.
- Use of compact models to demonstrate foundry device capabilities

Device Model Development

- Modeling of physical phenomena: Statistical variation, noise and fluctuations, RF and high-frequency effects, layout effects, etc.
- Methodologies to assist in model development, practices for coding, quality assurance, circuit simulator integration, etc.
- Parameter extraction, measurement techniques, model calibration, validation, and verification methodologies.

Model Enhancements and Implementations

- Model extensions to capture additional device features (leakage, capacitance, second-order dependencies) or expand the operating range of existing devices (bias, power, temperature, frequency, etc.)
- Model enhancements to support the design of new or demanding circuits
- Model workflow, implementation, and integration into the design environment (PDK)
- Computing/simulation platforms, simulation algorithms, and methodologies to improve simulation performance (parallel processing, etc.)
- Models for established device types that currently lack standardization.

Emerging devices

- Modeling of emerging and future devices: compact models for novel device technologies and architectures that could further revolutionize circuit performance and design flow. For example, complementary FET, ferroelectric devices, silicon photonics, MRAM, RRAM, cryogenic, quantum computing, 2D-materials, oxide semiconductors, etc.

IMPORTANT DATES

February 1, 2026
Submission deadline *(4-page paper)*

April 6, 2026
Acceptance notification

May 10, 2026
Final version for publication

July 30-31, 2026
Conference Takes Place

For more details visit: 2026.si2-icmc.org