Deep Cryogenic Operation of Single-Level and Stacked Nanowire and Nanosheet SOI MOSFETs for Quantum Computing

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Michelly de Souza is a Full Professor in the Electrical Engineering Department at Centro Universitário FEI, Brazil, and has been a CNPq Research Productivity Fellow since 2014. She holds a B.S. in Electrical Engineering from FEI, an M.S. and a Ph.D. from the Polytechnic School of the University of São Paulo (USP), and a specialization in School Management from USP. Her international experience includes research internships at the Université Catholique de Louvain, Belgium, and CEA-Leti, France.

With extensive expertise in nanoelectronics, Dr. Souza focuses on the electrical characterization, modeling, and simulation of CMOS semiconductor devices for high-performance and low-power integrated circuits. Her current research interests include the extreme-temperature performance of stacked nanowire and nanosheet SOI MOSFETs.

She is a permanent member of FEI's Graduate Program in Electrical Engineering, where she advises Master's and Ph.D. students. Throughout her career, she has coordinated numerous research projects funded by FAPESP and CNPq and has authored or co-authored over 200 papers in international journals and conferences.

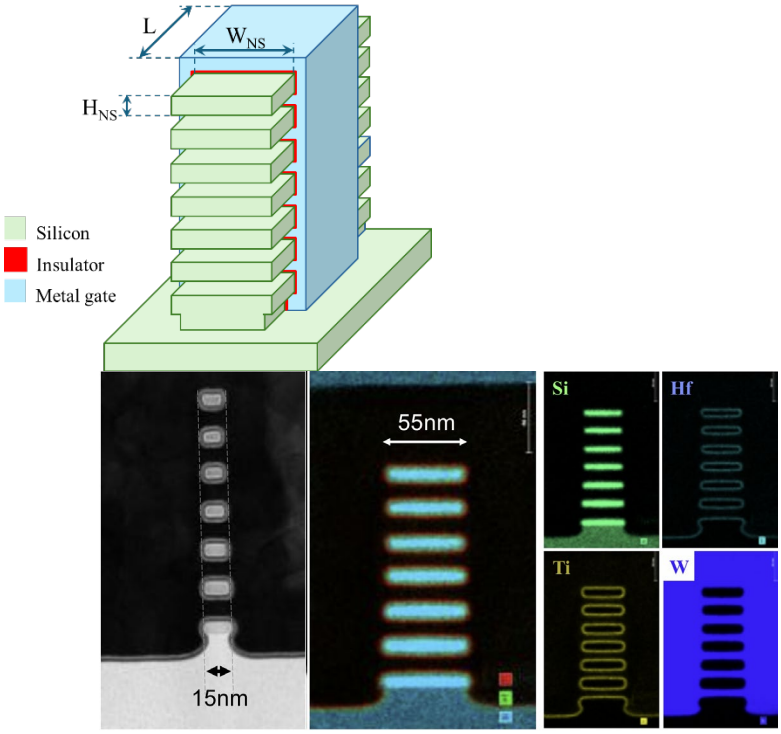
An IEEE Senior Member, she serves as the Counselor for the IEEE Student Branch at FEI and is a member of the Women in Electron Devices Society (WiEDS) committee. Additionally, she has held leadership roles in the Brazilian Microelectronics Society (SBMicro), serving as Administrative Director (2019–2022) and Financial Director (2022–2024).

Abstract:
The aggressive scaling of MOSFET dimensions triggered the search for alternative solutions for the traditional planar transistors for future technological nodes. Also, the advent of Quantum Computing raised interest in the cryogenic operation of ultimate MOSFETs for interface circuits between Qubits and electronic systems. Three-dimensional MOSFETs operating with fully depleted (FD) silicon fabricated in Silicon-On-Insulator (SOI) substrates are among the technological solutions being widely investigated.

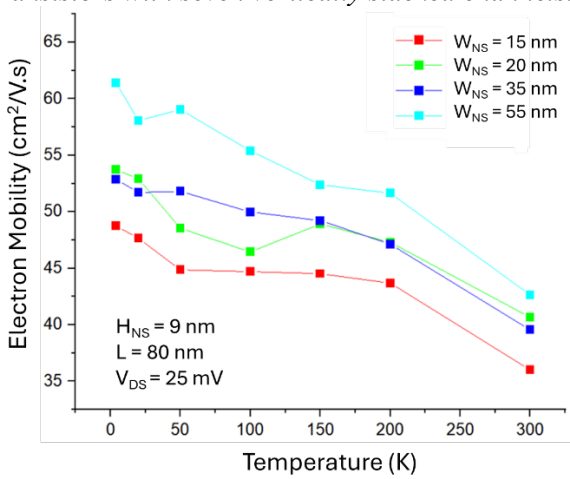
Triple-gate Ω-shaped MOSFETs with fin height and width of similar dimensions, in the order of 10-15nm, commonly referred to as nanowires (NWs) in the literature, are promising contenders. One key challenge in scaling down transistors is achieving high drive current density per footprint while simultaneously preserving the excellent electrostatics of nanometer-scale MuGFETs, which is crucial for mitigating short-channel effects. To address these scaling limitations, vertically stacked nanosheet transistors have attracted considerable attention. By layering multiple channels on top of each other, it allows for a

significant increase in the current level per unit area, without sacrificing the electrostatic integrity inherently provided by nanometric MuGFETs. The experimental demonstration of seven-level stacked gate-all-around (GAA) nanosheet transistors achieved significant performance enhancements in both digital and analog applications, surpassing single-level transistors with similar structural characteristics. Moreover, due to their nanometer-scale channels, quantum transport can be observed in aggressively scaled nanowires at cryogenic temperatures.

In this scenario, this talk will present and discuss the operation of nanowire transistors, both single-level and stacked with up to seven levels, when exposed to cryogenic temperatures down to 4 K. Peculiarities of these devices while operating in the cryogenic regime, such as transconductance oscillations indicating carrier confinement and self-heating, will be presented.



Schematic three-dimensional representation, TEM and EDS spectroscopy images of nanosheet transistors with seven vertically stacked channels.



Extracted carrier mobility of seven-level stacked nanosheet SOI transistors down to 4K.